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Supplementary Materials for

Reconfigurable ferroelectric transistor array for embodied neuromorphic vision with hardware-native sensing, computing, and activation

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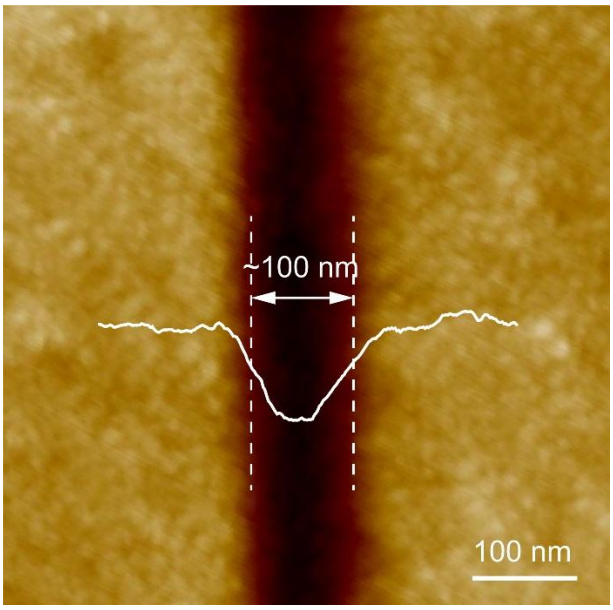


Fig. S1 AFM image of the split MLG control gates. AFM image showing the nanogap between dual MLG control gates after focused ion beam (FIB) cutting. The separation between the two gates is approximately 100 nm, as confirmed by the cross-sectional profile.

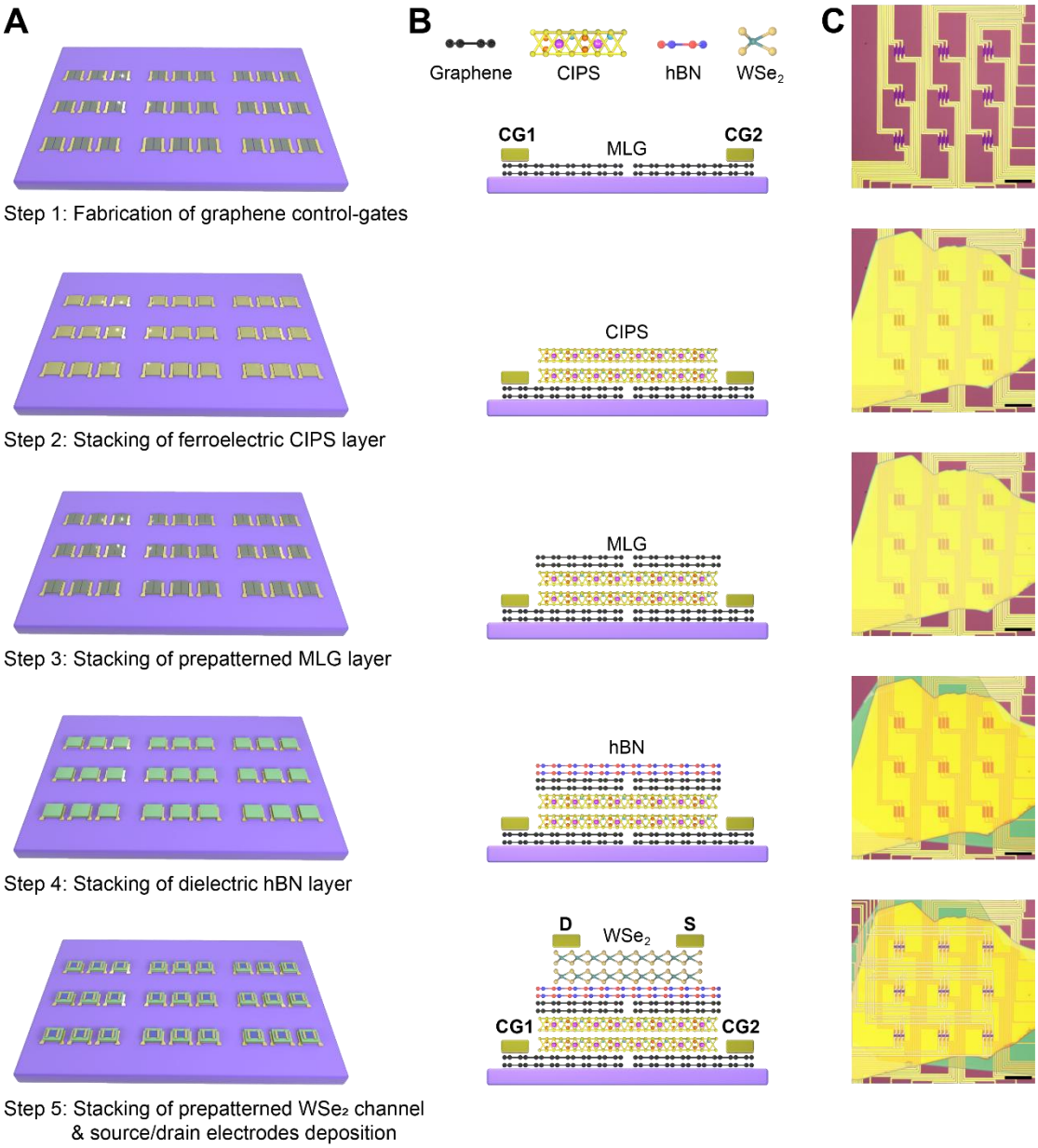


Fig. S2 Fabrication processes of the MFMIS-structure Fe-FET array. (**A**) Schematic illustration of the five fabrication steps. Step 1: Multilayer graphene (MLG) was mechanically exfoliated onto a SiO_2/Si substrate and patterned into a 3 × 3 × 3 array using femtosecond laser micromachining. Each MLG flake was then split into two parts by FIB cutting to form dual control gates (CG1 and CG2) with approximately 100 nm spacing. Cr/Au (10 nm/50 nm) electrodes were deposited via electron beam lithography (EBL) and evaporation to connect the MLG gates. Step 2: A mechanical exfoliated ferroelectric CISP flake (~80 nm thickness) was transferred to cover the entire MLG array. Step 3: A separate MLG flake was patterned into a 3 × 3 × 3 split-square array and aligned precisely atop the CIPS layer to form the MLG/CIPS/MLG ferroelectric capacitor. Step 4: A dielectric hBN flake (~13 nm thickness) was stacked to isolate the MLG/CIPS/MLG heterostructure. Step 5: An ambipolar WSe_2 flake (~5

nm thickness) was exfoliated and patterned into a 3 × 3 × 3 array, aligned above the hBN layer to serve as the channel material. Cr/Au (10 nm/50 nm) source/drain electrodes were deposited on the WSe_2 channel using EBL and evaporation. Noteworthily, the conductive components in the array, including WSe_2 channels, the MLG control gates and interlayers, are patterned into isolated arrays to eliminate lateral electrical connection between neighboring pixels. (**B**) Layer-by-layer schematic cross-sections illustrating the material stacking and electrode configuration at each fabrication stage. (**C**) Optical images of the array structure after each key fabrication step, corresponding to the illustrations in (**A**). Scale bars, 30 μm.

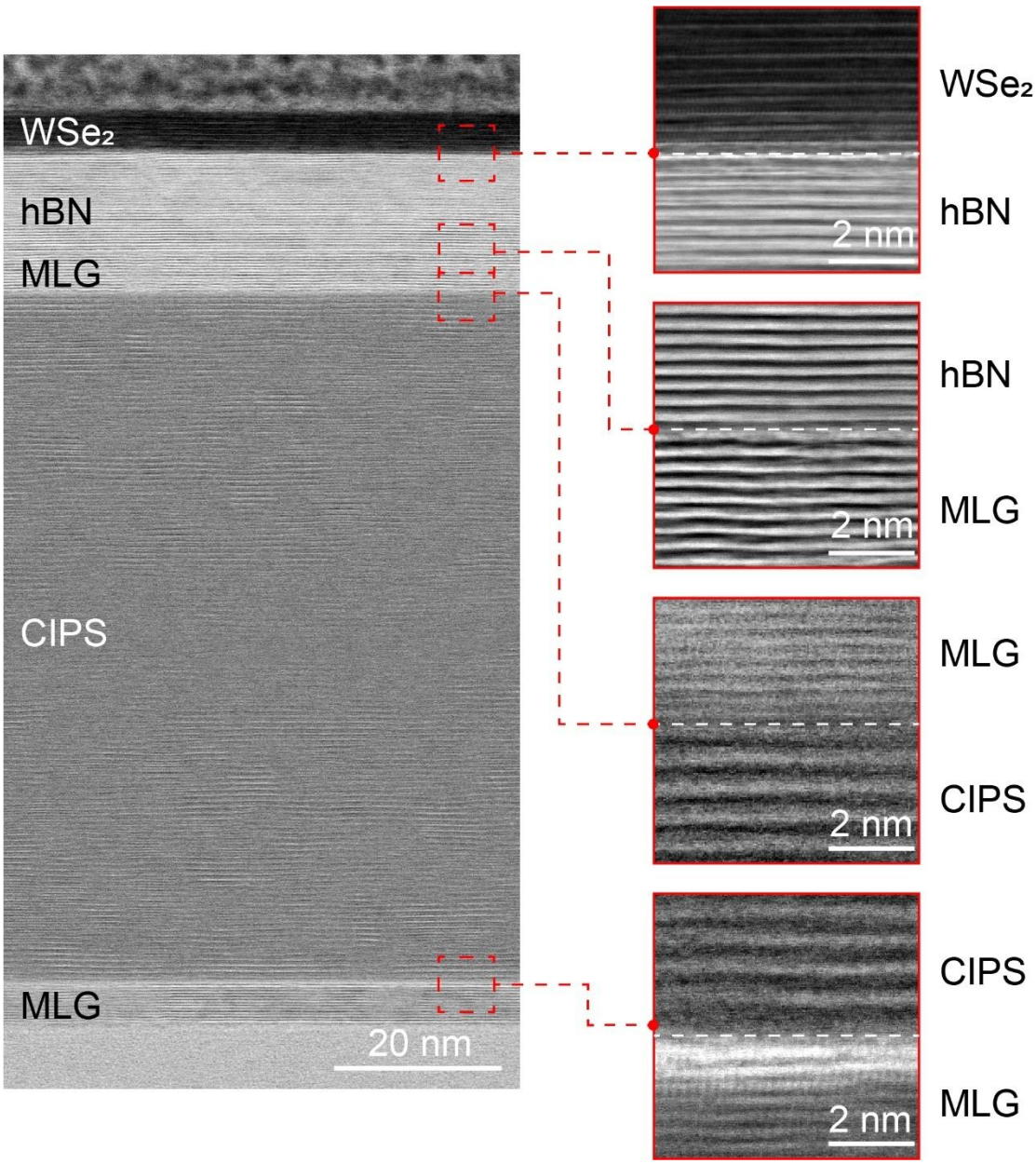


Fig. S3 Cross-sectional STEM image of the MFMIS-structure Fe-FET. High-resolution cross-sectional scanning transmission electron microscopy (STEM) image of the multilayer Fe-FET device, showing the vertically stacked architecture comprising WSe_2, hBN, MLG, ferroelectric CIPS, and bottom MLG gate layers. Enlarged panels on the right highlight the well-defined interfaces between adjacent layers, confirming the integrity and cleanliness of the van der Waals heterostructure.

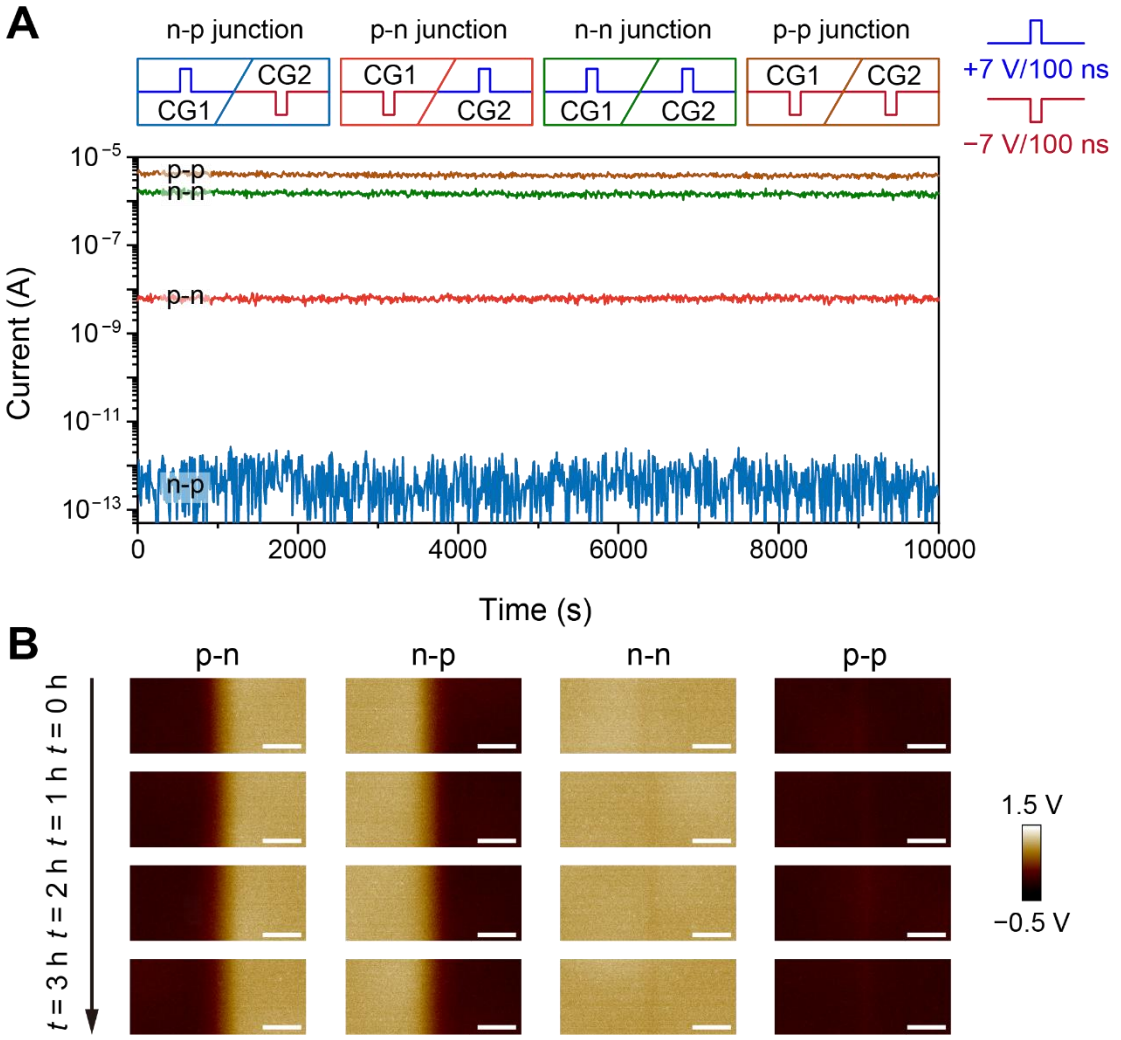


Fig. S4 Long-term retention of the Fe-FET under different homojunction configurations. (**A**) Retention characteristics of the MFMIS-structure Fe-FET programmed into four homojunction states: n–p, p–n, n–n, and p–p. The top schematics illustrate the gate voltage (V_G) pulse configurations applied to CG1 and CG2 to program each state, where blue and red waveforms represent +7 V/100 ns and –7 V/100 ns pulses, respectively. After programming, the drain current (I_{ds}) was measured over 10,000 s under a constant V_{ds} = 0.5 V to evaluate state retention. (**B**) Kelvin probe force microscopy (KPFM) images of the Fe-FET in the four junction configurations, recorded at t = 0, 1, 2, and 3 h. The persistent surface potential contrast confirms that the programmed homojunction states remain stable over time without external gate bias. Scale bars, 500 nm.

Supplementary Note 1. Configurations of the Fe-FET for sensor mode and synapse mode

1.1 Sensor mode configuration for ISC

In the sensor mode, the Fe-FET operates as a self-powered photodetector capable of ISC. The key mechanism relies on the programmable formation of internal p–n or n–p homojunctions, induced by antiparallel polarization states in the two lateral CIPS regions. These ferroelectric polarization states modulate the local electrostatic potential in the WSe_2 channel, creating a built-in electric field without requiring external gate bias. This field drives the separation of photogenerated electron–hole pairs under broadband illumination, producing a photovoltaic current that reflects both the spatial distribution of ferroelectric polarization and the local light intensity.

As schematically illustrated in fig. S5 (A and B), when the left and right CIPS layers are polarized in opposite directions (e.g., left-down and right-up for a p–n configuration, or vice versa for n–p), the resulting built-in electric field points laterally across the channel, enabling efficient and directional charge separation. The output *I–V* characteristics (fig. S5C) exhibit rectifying behavior, with the polarity and magnitude of the short-circuit current (I_{sc}) determined by the junction configuration. Notably, I_{sc} at zero bias serves as a direct measure of the device's photoresponsivity, which can be continuously tuned in both magnitude and polarity by reprogramming the ferroelectric states.

To demonstrate this tunability, we created seven intermediate junction states (I–VII) by stepwise modulation of the polarization configurations, spanning from n–p to p–n. As shown in the KPFM images in fig. S5D, the surface potential undergoes a gradual reversal. Correspondingly, the device exhibits a smooth transition in *I–V* characteristics and short-circuit current polarity (fig. S5E). This confirms the device’s ability to realize analog, reconfigurable photoresponsivity states across a continuous range.

In the context of ISC, the polarization-programmed photoresponsivity *R* of each Fe-FET effectively emulates the weight in a neural network, while the incident light intensity *P* serves as the input signal. By connecting multiple Fe-FETs in parallel, the

total photocurrent follows Kirchhoff's law and accumulates linearly as $I_{ph} = P_1R_1 + P_2R_2 + \ldots + P_nR_n$, enabling multiply-accumulate (MAC) operations directly in the sensor array. Furthermore, by arranging multiple subpixels within each pixel (e.g., 3 × 3), matrix–vector multiplication (MVM) can be achieved in a spatially parallel fashion, where each subpixel of the array outputs an analog-weighted sum corresponding to one projection of the input (*6*). This hardware-native realization of MVM at the sensor layer forms the basis for real-time convolution, spatial filtering, and encoding in neuromorphic vision systems.

Importantly, both the junction profile and photoresponsivity are non-volatile and electrically reprogrammable, owing to the stable remanent polarization of the CIPS layers. This allows zero-standby-power operation and persistent weight storage without auxiliary memory or bias circuitry—distinguishing this ISC platform from conventional photodetectors and enabling compact, energy-efficient architectures for intelligent perception at the edge.

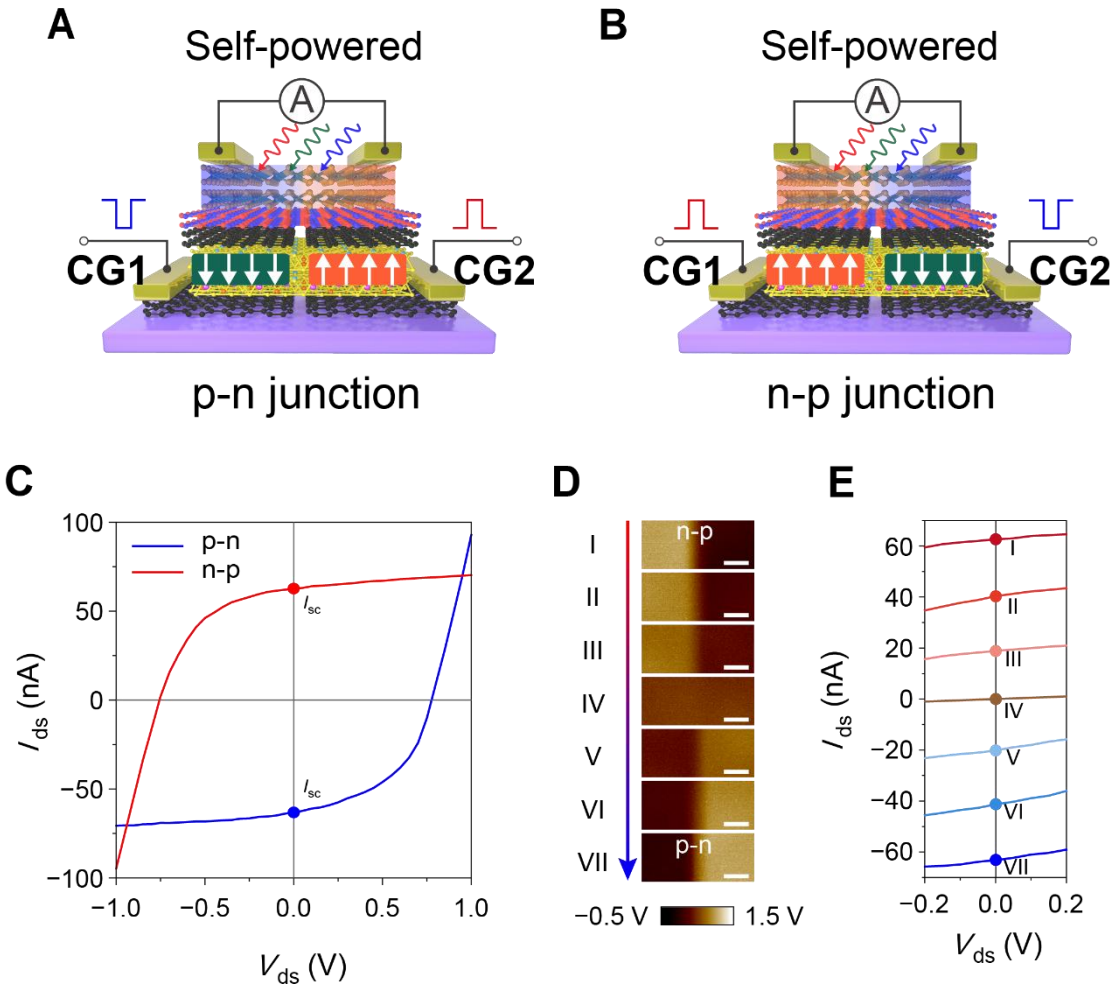


Fig. S5 Sensor mode of the Fe-FET with tunable photoresponsivity for ISC. (**A** and **B**) Schematic illustrations of the Fe-FET operating in self-powered sensor mode under p–n (**A**) and n–p (**B**) configurations. The local built-in electric field, arising from antiparallel polarization of the two CIPS regions, drives the separation of photogenerated carriers under broadband illumination, enabling polarity-dependent photocurrent generation. (**C**) *I-V* characteristics of the device under illumination in p–n (blue) and n–p (red) configurations. Both exhibit clear rectifying behavior with opposite polarities. The blue and red dots at zero bias correspond to the short-circuit currents (I_{sc}) for each configuration, reflecting the switchable photovoltaic response. (**D**) KPFM images of seven programmable junction states (I–VII), illustrating the gradual reversal of internal potential from n–p to p–n configurations via stepwise modulation of CIPS polarization. Scale bars, 500 nm. (**E**) Corresponding *I-V* curves under illumination for each state. The current values at V_{ds} = 0 V indicate the I_{sc} of each configuration, showing continuous and bidirectional tuning of photocurrent magnitude and polarity across the seven programmable states.

1.2 Synapse mode configuration for IMC

In synapse mode, the Fe-FET operates as a reconfigurable memory element with analog conductance tunability, suitable for IMC operations such as MAC and MVM. The key mechanism lies in spatially selective ferroelectric polarization control within the CIPS layers, which modulates the local junction profile and charge transport in the WSe_2 channel.

To initialize the device for synaptic weight programming, a preset voltage pulse of –7 V/100 ns is first applied to CG2, polarizing the right-side CIPS region downward. This induces strong hole accumulation in the adjacent WSe_2 channel, setting the drain side into a stable p^+-type state. After this step, CG2 is left floating to preserve the remanent polarization. This fixed p^+ region ensures a consistent reference state for subsequent modulation.

Programming of the left-side polarization—and thus the junction configuration—is then performed by applying a sequence of positive or negative voltage pulses to CG1. Positive pulses drive the left CIPS region into the upward polarization state, forming an n–p^+ junction with a strong rectifying barrier that suppresses channel current. This n–p^+ state defines the off-state of the device (fig. S6A). Conversely, negative pulses switch the left region upward, eventually forming a p^+–p^+ junction with high conductance (fig. S6B).

As shown in fig. S6C, the conductance contrast between the high-conductance p–p and low-conductance n–p states exceeds 10^7 at a read voltage of 0.1 V. Importantly, fine-tuning of the polarization amplitude in the left CIPS region allows gradual modulation of the channel conductance, enabling analog-like behavior across multiple intermediate p^-–p^+ configurations (fig. S6D). This analog conductance serves as a non-volatile and electrically programmable synaptic weight.

In IMC implementations, a voltage vector $\boldsymbol{V} = [V_1, V_2, ..., V_n]$ is applied across a synapse array, and each device's conductance G_i modulates the corresponding current response I_i. According to Ohm's law and Kirchhoff's current law, the total output current I_{out} is given by:

$$I_{\text{out}} = \sum_i V_{\text{i}} G_{\text{i}} ,$$

realizing linear MAC operations directly in the analog domain without digital multiplication or external memory access.

The combination of high dynamic range, non-volatility, and local reconfigurability in the Fe-FET platform makes it an effective synaptic primitive for neuromorphic hardware, enabling fast, low-power, and densely integrated IMC functionality.

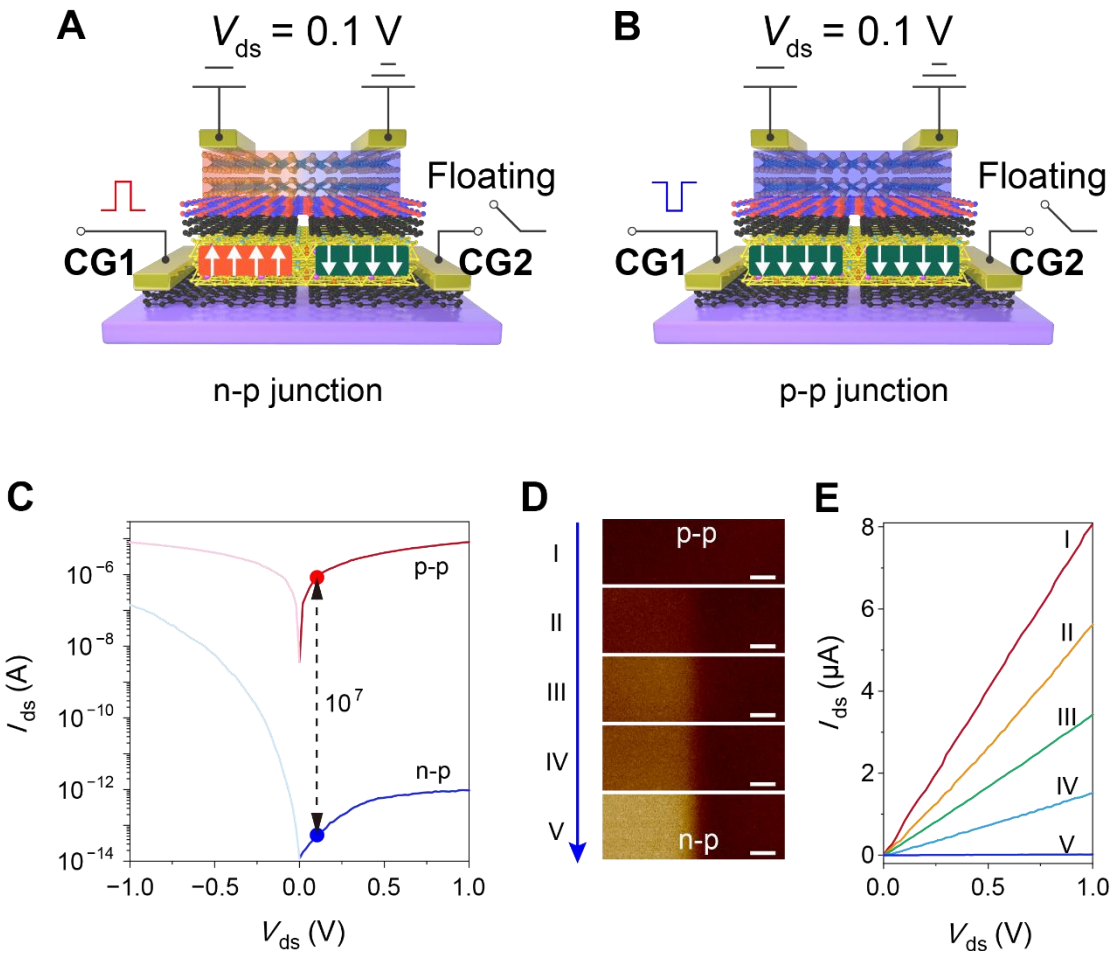


Fig. S6 Synapse mode of the Fe-FET with tunable conductance for IMC. (**A** and **B**) Schematic illustrations of the Fe-FET operating in synapse mode under n–p (**A**) and p–p (**B**) configurations. During programming, a voltage pulse is applied to CG1 while CG2 is left floating, selectively switching the polarization state of the left CIPS region. The resulting junction configuration modulates the carrier transport in the WSe_2 channel, determining the conductance under a small read voltage (V_{ds} = 0.1 V). (**C**) *I*–*V* characteristics of the Fe-FET under n–p (blue) and p–p (red) configurations. A conductance switching ratio exceeding 10^7 is achieved at 0.1 V, providing a well-defined on/off contrast between logic states. (**D**) KPFM images of the device under five intermediate polarization states (I–V), demonstrating the gradual evolution from a high-conductance p^+–p^+ channel (I) to a low-conductance n–p junction (V). The surface potential contrast reflects the built-in electric field modulation induced by spatially reconfigured ferroelectric polarization, which governs the carrier transport behavior in the WSe_2 channel. Scale bars, 500 nm. (**E**) Corresponding *I*–*V* curves for the five states in d, confirming analog, monotonic conductance tuning under forward bias. The continuously adjustable current levels serve as electrically programmable synaptic weights in IMC architectures.

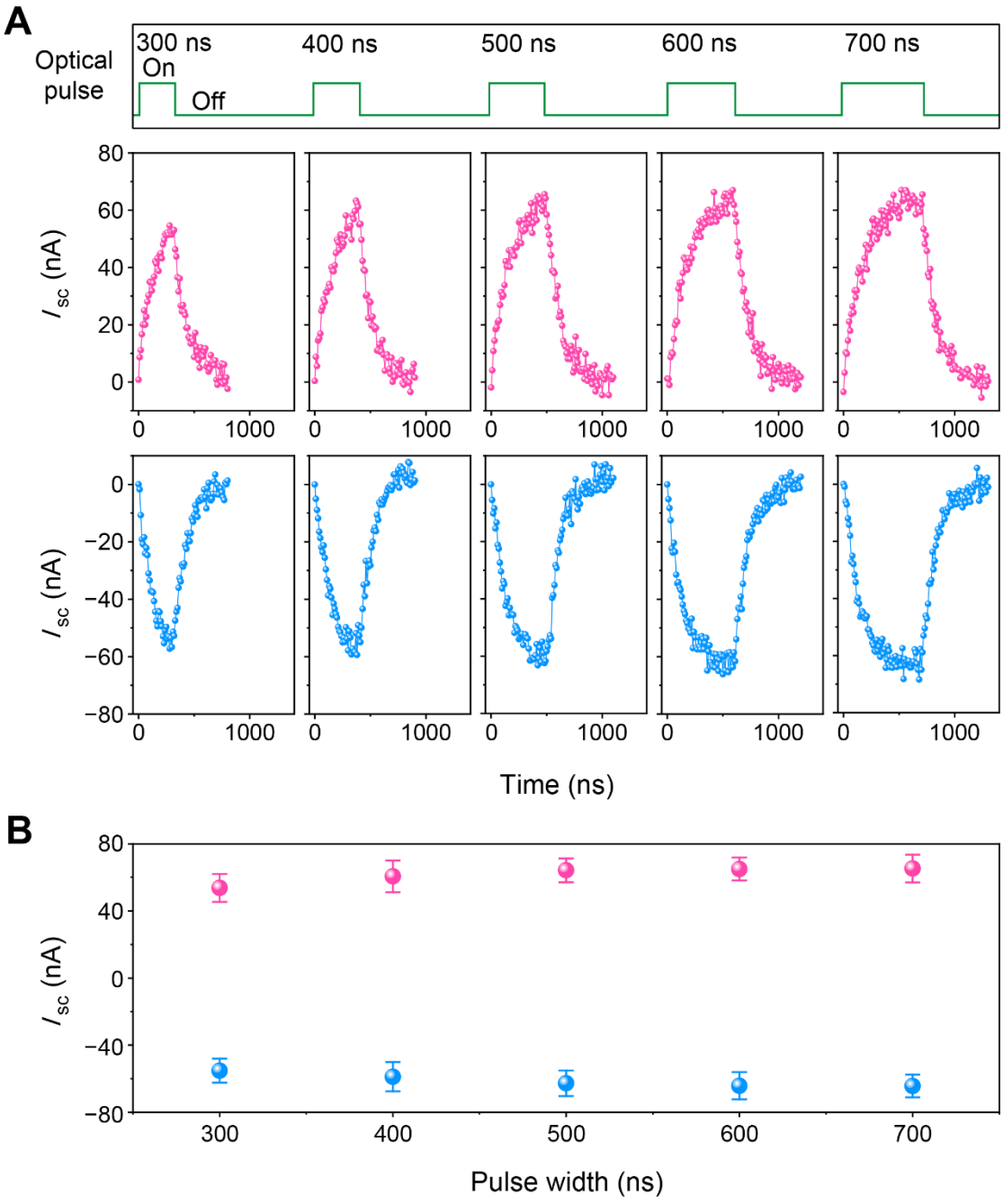


Fig. S7 Nanosecond photoresponse dynamics of the Fe-FET in sensor mode for high-speed ISC. (**A**) Transient short-circuit photocurrents (I_{sc}) of the Fe-FET with positive (pink) and negative (blue) photoresponsivity under optical pulses of varying widths (300–700 ns). The optical pulse waveform is shown at the top. Devices were programmed to ±160 mA W^{-1} photoresponsivity, and the resulting I_{sc} was recorded with nanosecond resolution. (**B**) Extracted peak photocurrents corresponding to each pulse width, confirming consistent and high-speed photoresponse for both polarities. These results demonstrate the Fe-FET's capability for nanosecond optical sensing and polarity-reconfigurable response, supporting high-speed ISC operations.

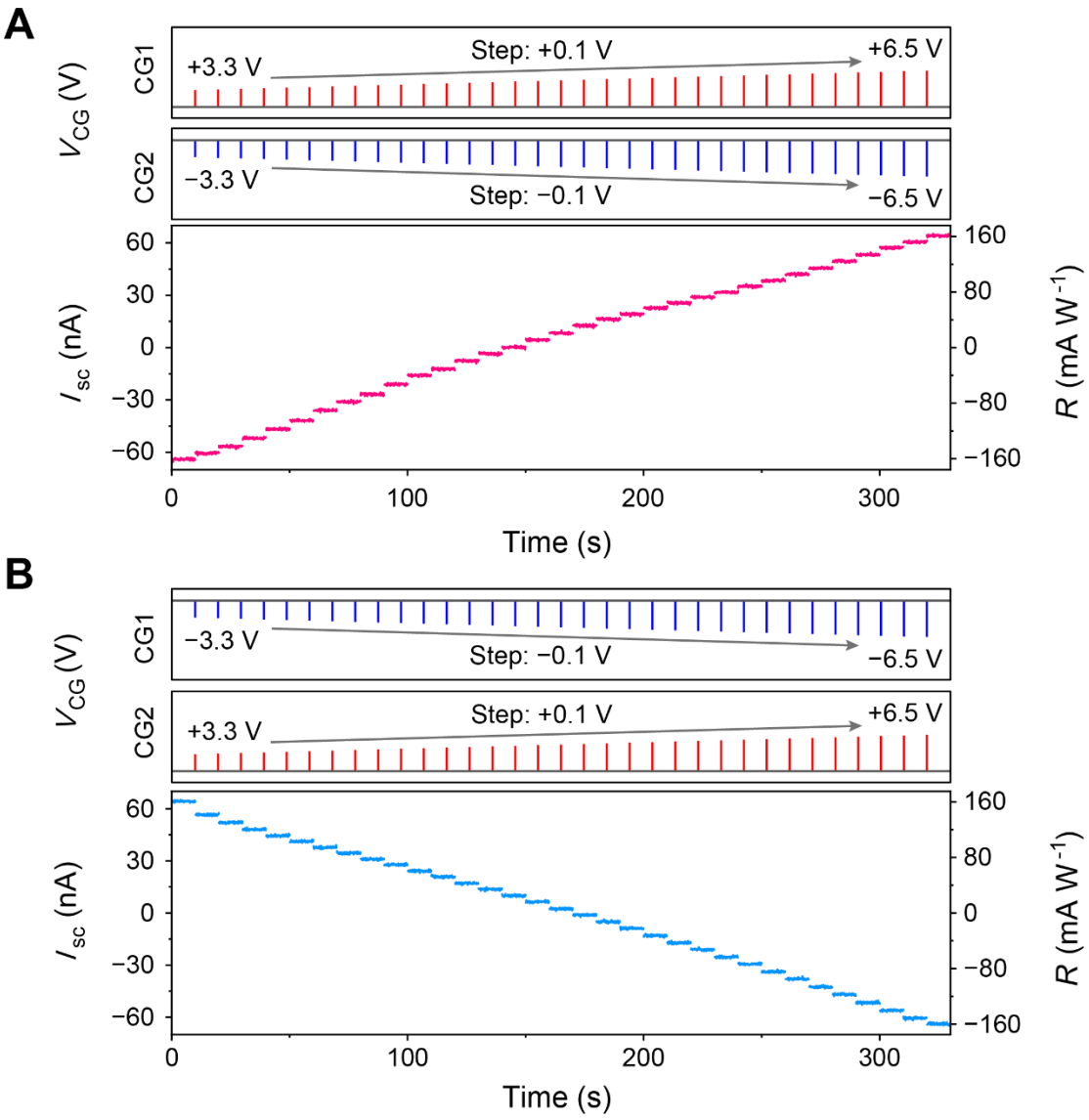


Fig. S8 Symmetric and linear updating of photoresponsivity in positive and negative regimes. (**A** and **B**) Analog tuning of the Fe-FET's photoresponsivity across 33 discrete levels within a dynamic range of ±160 mA W^{-1}, measured via the short-circuit photocurrent (I_{sc}) under illumination. The corresponding photoresponsivity (R) is calculated and shown on the right axis. Top panels depict the gate pulse schemes used for photoresponsivity updating. In LTP mode (**A**), a series of positive voltage pulses (from +3.3 V to +6.5 V in 0.1 V steps, 100 ns duration) were applied to CG1, while simultaneously applying negative pulses of equal amplitude and duration to CG2. In LTD mode (**B**), an inverse scheme was used: CG1 received negative pulses (–3.3 V to –6.5 V), and CG2 received positive pulses (from +3.3 V to +6.5 V) with the same increment and duration. The symmetric and gradual modulation of I_{sc} validates the Fe-FET's capability for analog and bidirectional photoresponsivity tuning, essential for weight updates in ISC and hybrid neuromorphic systems.

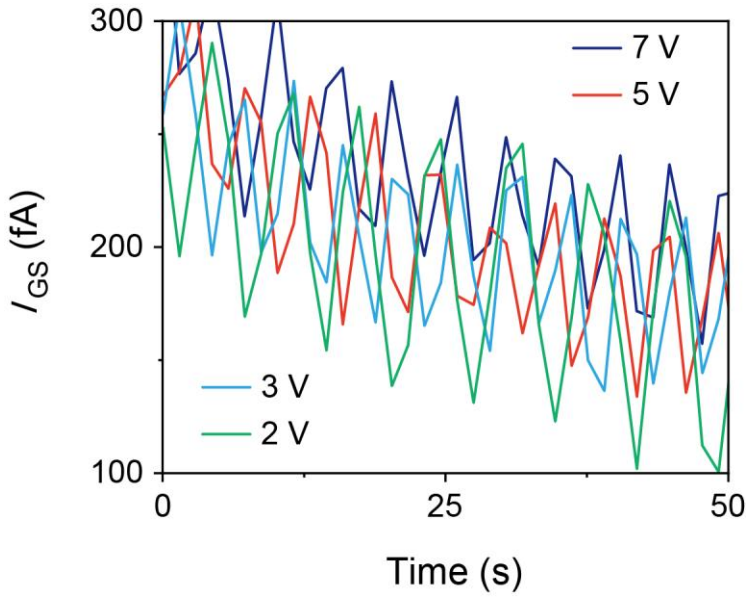


Fig. S9 Gate leakage characteristics of the MFMIS-structure Fe-FET. Gate leakage currents (I_{GS}) were measured under continuous gate bias from 2 V to 7 V, with both source and drain terminals grounded. The leakage current remained in the sub-picoampere range (~100–300 fA), indicating excellent gate insulation.

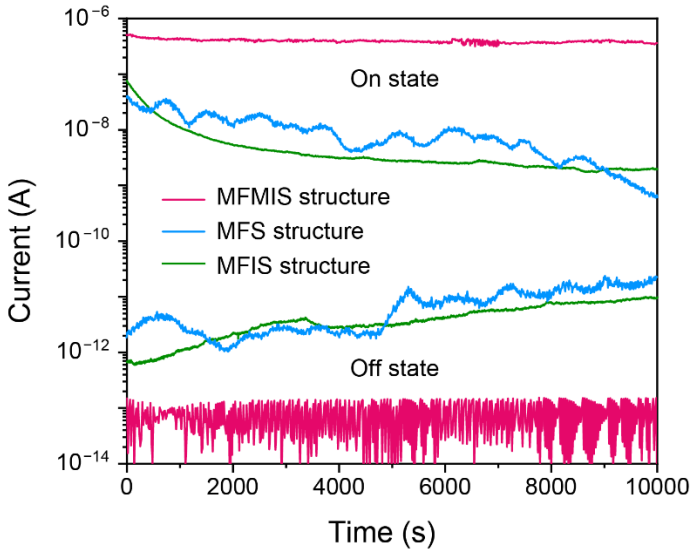


Fig. S10 Retention performance comparison of MFMIS, MFS, and MFIS Fe-FET structures. Time-dependent current measurements of the on and off states over 10^4 seconds for Fe-FETs with three different gate stack configurations: MFMIS (pink), MFS (blue), and MFIS (green). The MFMIS-structure device exhibits superior non-volatile retention in both on and off states, with negligible current degradation, while the MFS and MFIS counterparts show significant current drift due to depolarization effects and charge instability. These results highlight the importance of the MFMIS architecture for achieving reliable memory behavior and long-term data retention in reconfigurable neuromorphic systems.

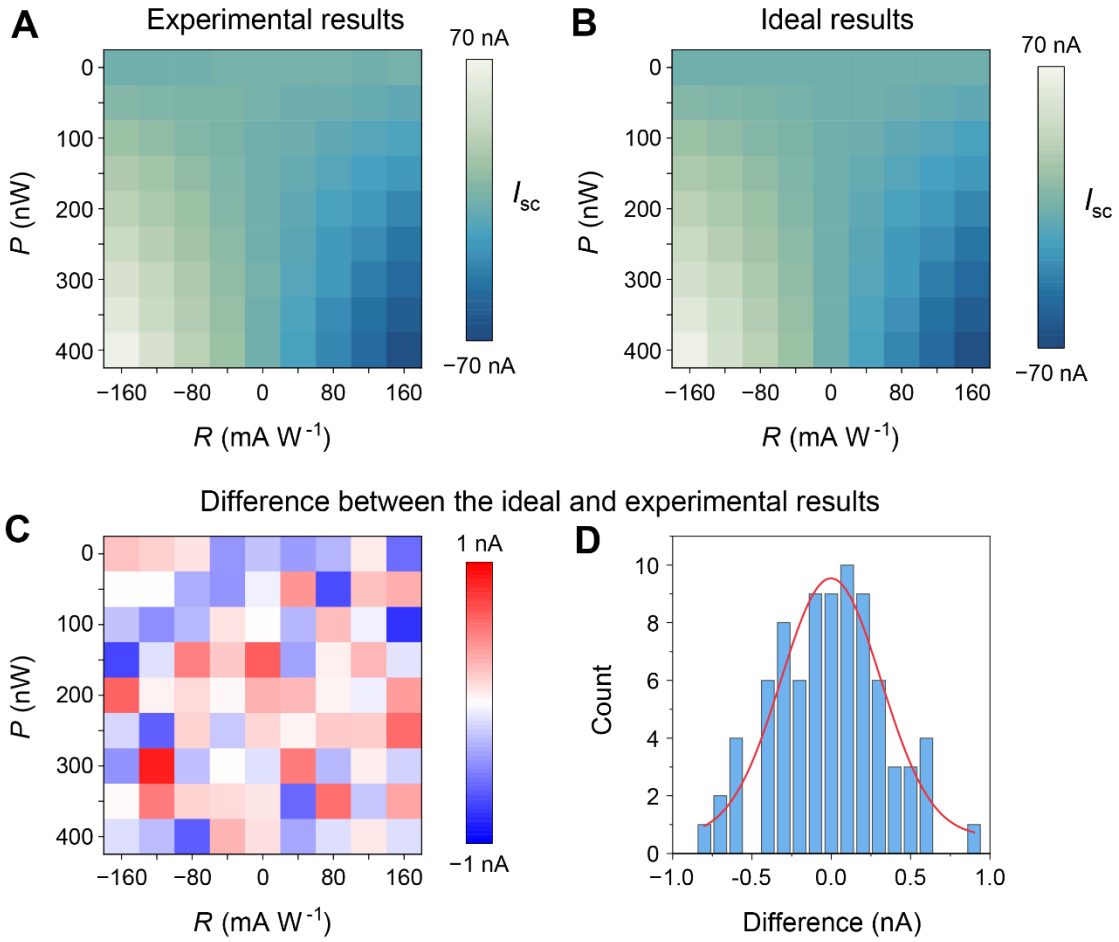


Fig. S11 Precision of analog–analog multiplication in ISC mode. (**A** and **B**) Comparison between experimentally measured (**A**) and theoretically ideal (**B**) short-circuit photocurrents I_{sc} generated by multiplying input light intensity P and programmable photoresponsivity R across a range of values (–160 to +160 mA W^{-1}, 0–400 nW). (**C**) Pixel-wise difference between the measured and ideal values, illustrating a maximum error below ±1 nA, confirming high-accuracy analog multiplication. (**D**) Histogram of the differences shown in (**C**) with a fitted Gaussian curve, demonstrating centered and narrow distribution with minimal deviation, validating the robustness and linearity of the Fe-FET-based analog MAC operation.

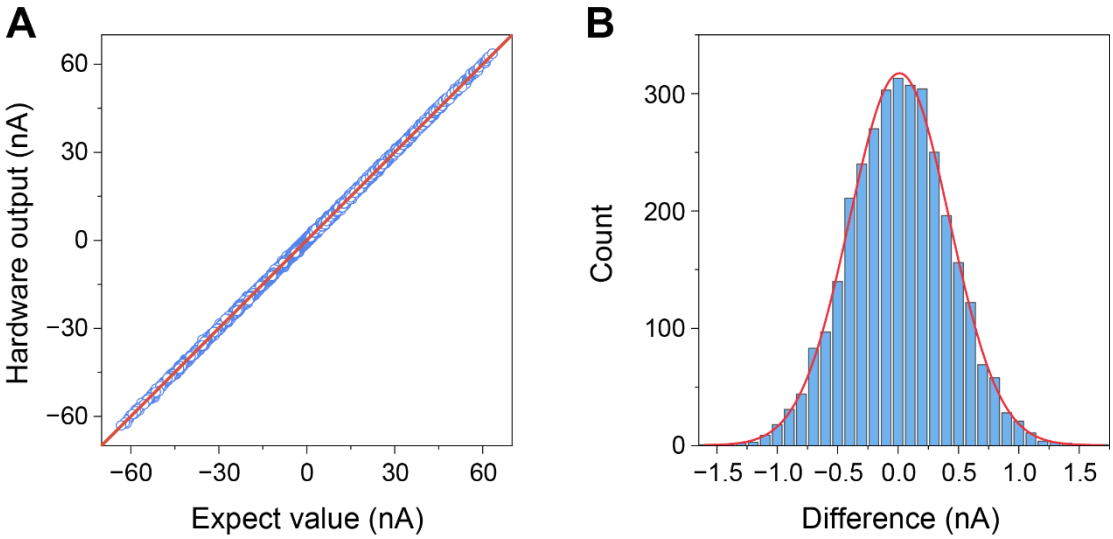


Fig. S12 Statistical evaluation of analog–analog multiplication accuracy across randomized input intensity and photoresponsivity. (**A**) Correlation plot between experimentally measured hardware output currents and expected values computed as the product of randomly selected photoresponsivity and light intensity (N = 1000). The red diagonal line represents ideal correspondence. The close alignment of data points to the ideal line confirms high fidelity of analog multiplication. (**B**) Histogram of current differences between hardware and ideal outputs. The distribution is well-fitted by a Gaussian profile centered near zero, with most deviations confined within ±1.5 nA, indicating excellent linearity, reproducibility, and noise resilience of the ISC-based analog MAC computation.

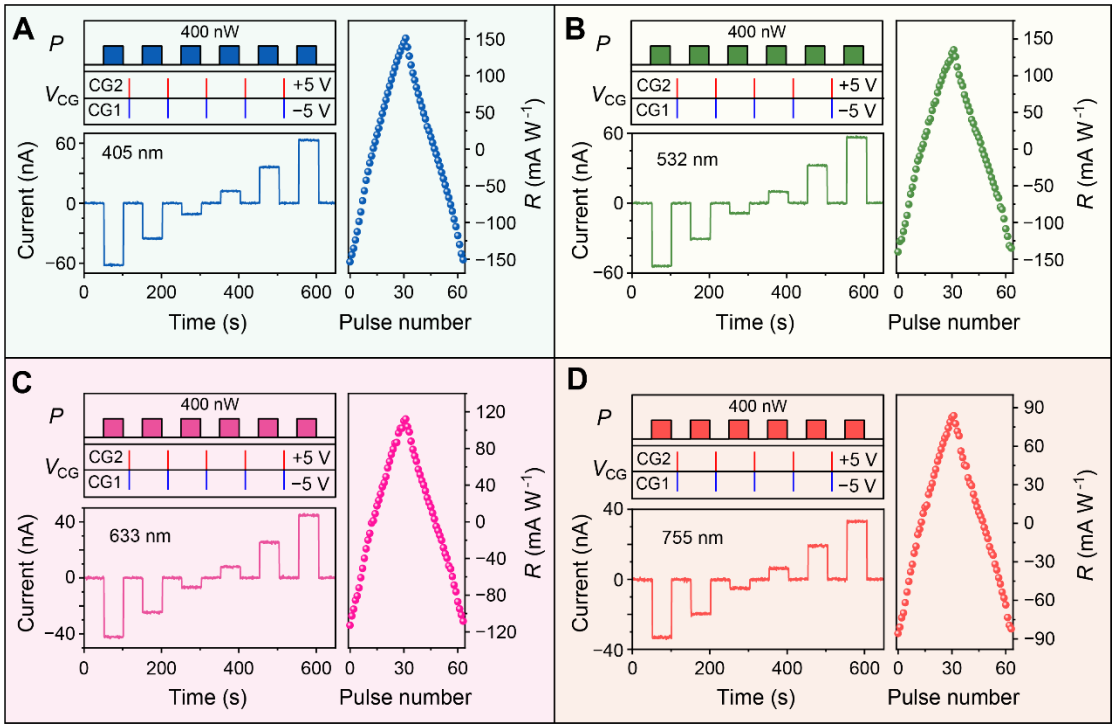


Fig. S13 Broadband photoresponse and programmable photoresponsivity of the sensor-mode Fe-FET. (**A**–**D**) Photocurrent responses of the Fe-FET operated in sensor mode under pulsed illumination with wavelengths of 405 nm (**A**), 532 nm (**B**), 633 nm (**C**), and 755 nm (**D**), respectively. The incident optical power was fixed at 400 nW. For each wavelength, ±5 V/100 ns voltage pulses were alternately applied to CG1 and CG2 to modulate the ferroelectric polarization states of the CIPS layers, thereby tuning the photoresponsivity (*R*) of the device. Left panels show the time-resolved photocurrents (I_{sc}) under light pulses, while right panels plot the photoresponsivity updating behaviors at corresponding wavelength. The Fe-FET demonstrates reliable and reversible photoresponse tuning across the entire visible range, confirming its broadband applicability for in-sensor computing tasks.

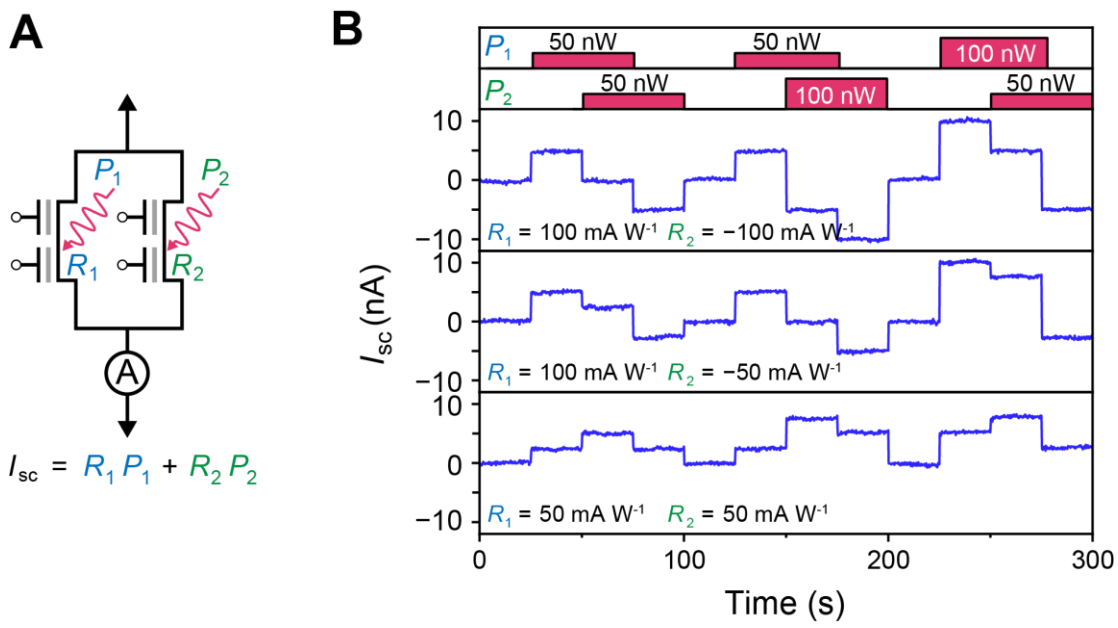


Fig. S14 Photocurrent accumulation in two parallel-connected sensor-mode Fe-FETs. (**A**) Schematic of a parallel circuit comprising two Fe-FETs configured in sensor mode. Each device is independently programmed into a p–n or n–p state with corresponding photoresponsivities R_1 and R_2, and illuminated by light intensities P_1 and P_2, respectively. Under short-circuit conditions, the total photocurrent I_{sc} is given by $I_{sc} = R_1P_1 + R_2P_2$. (**B**) Measured total photocurrent generated by the two Fe-FETs under varying combinations of P_1 and P_2. The three panels correspond to different programmed photoresponsivities (R_1 and R_2) of (100, –100), (100, –50), and (50, 50) mA W^{-1}, respectively. The measured output closely follows the predicted linear accumulation of photoresponses from each device, confirming that both positive and negative photocurrents can be directly summed without the need for dark current subtraction—an essential feature for reliable and efficient analog MVM in ISC architectures.

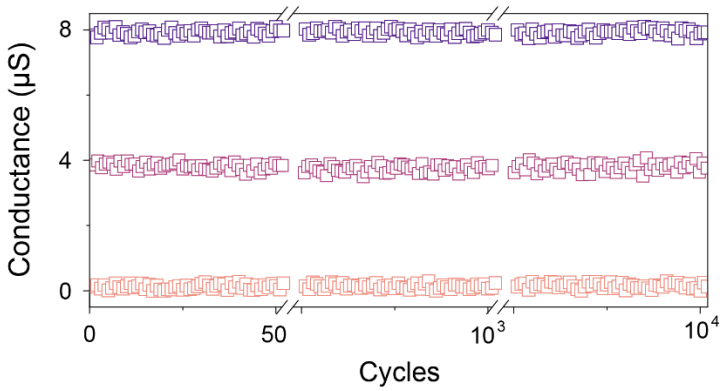


Fig. S15 Stable endurance of conductance states in synapse-mode Fe-FET over 10^4 update cycles. Conductance retention of three representative programmable conductance states (0, 4, and 8 μS) under repeated write–read cycles. The Fe-FET exhibits excellent stability and minimal degradation across 10,000 electrical updates, confirming its reliable endurance performance for synaptic weight storage in IMC tasks.

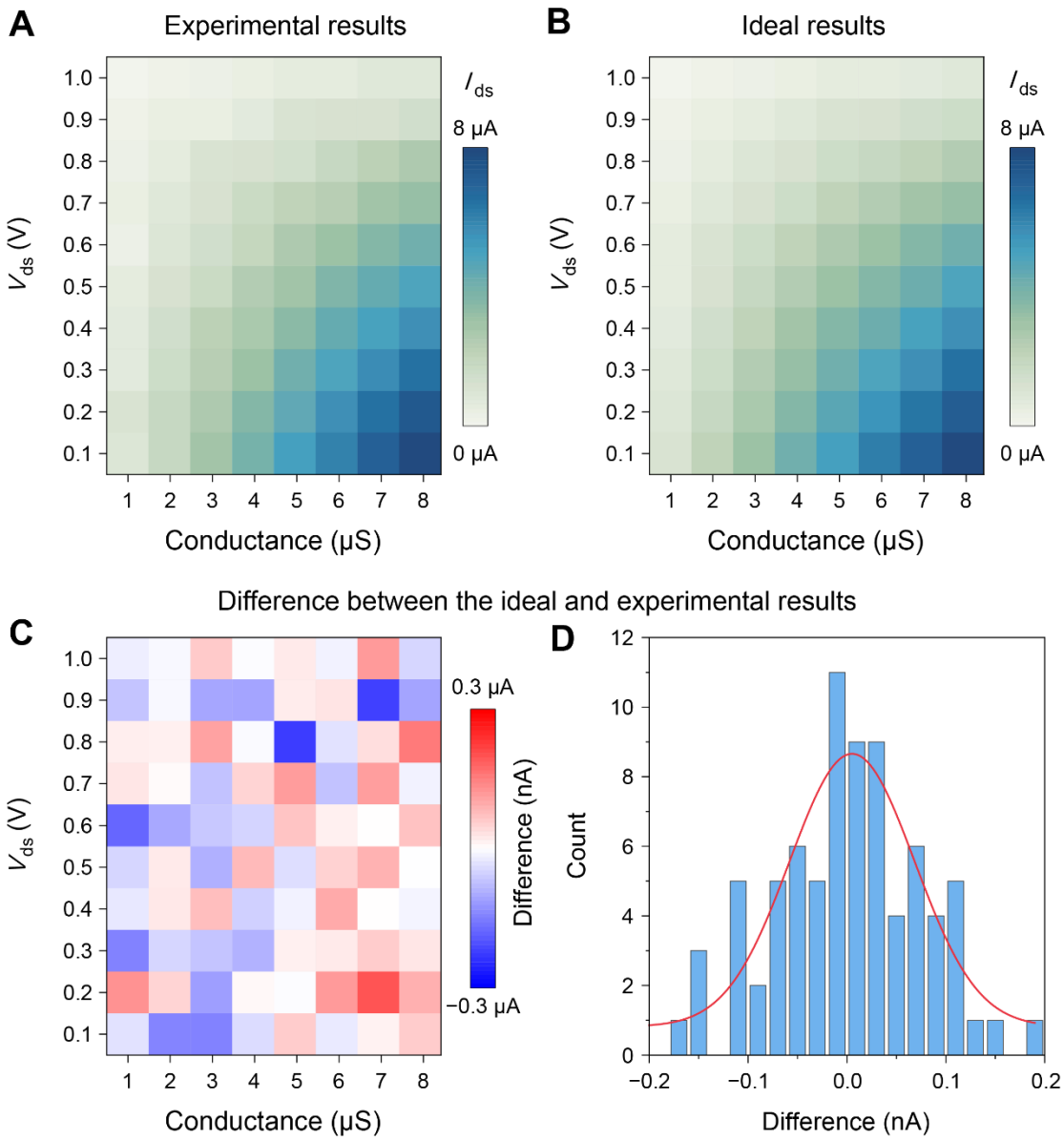


Fig. S16 Precision of analog–analog multiplication in IMC mode. (**A** and **B**) Comparison between experimentally measured (**A**) and theoretically ideal (**B**) output current generated by multiplying input voltage (V_{ds} = 0.1–1.0 V) and programmable conductance (1–8 μS). (**C**) Pixel-wise difference map between experimental and ideal results, with all deviations confined within ±0.3 μA, validating high-precision analog MAC execution. (**D**) Histogram of the current differences in (**C**), fitted with a Gaussian curve, indicating a centered distribution with standard deviation <0.1 μA, confirming the linearity, accuracy, and reliability of the Fe-FET-based analog computing platform.

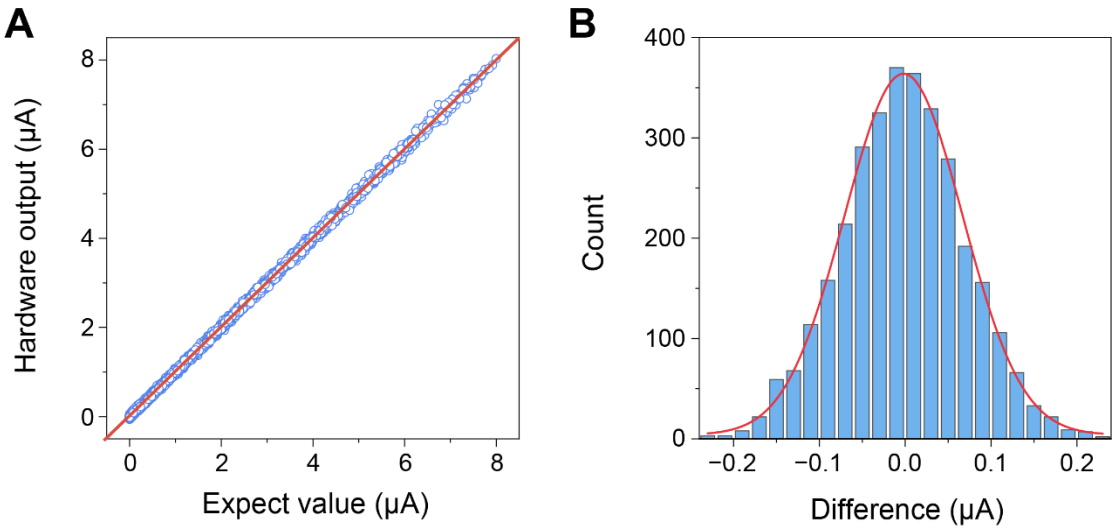


Fig. S17 Statistical evaluation of analog–analog multiplication accuracy across randomized input voltage and conductance. (**A**) Correlation between experimentally measured hardware output currents and expected values, computed from 1000 random combinations of input voltage and conductance. The red diagonal represents the ideal correspondence. The close clustering of data points along the line confirms the high fidelity of the analog MAC operation. (**B**) Histogram of the current differences between experimental and ideal results. The distribution follows a Gaussian profile centered around zero, with over 95% of values falling within ±0.2 μA, demonstrating excellent linearity, stability, and noise tolerance of the Fe-FET–based IMC architecture.

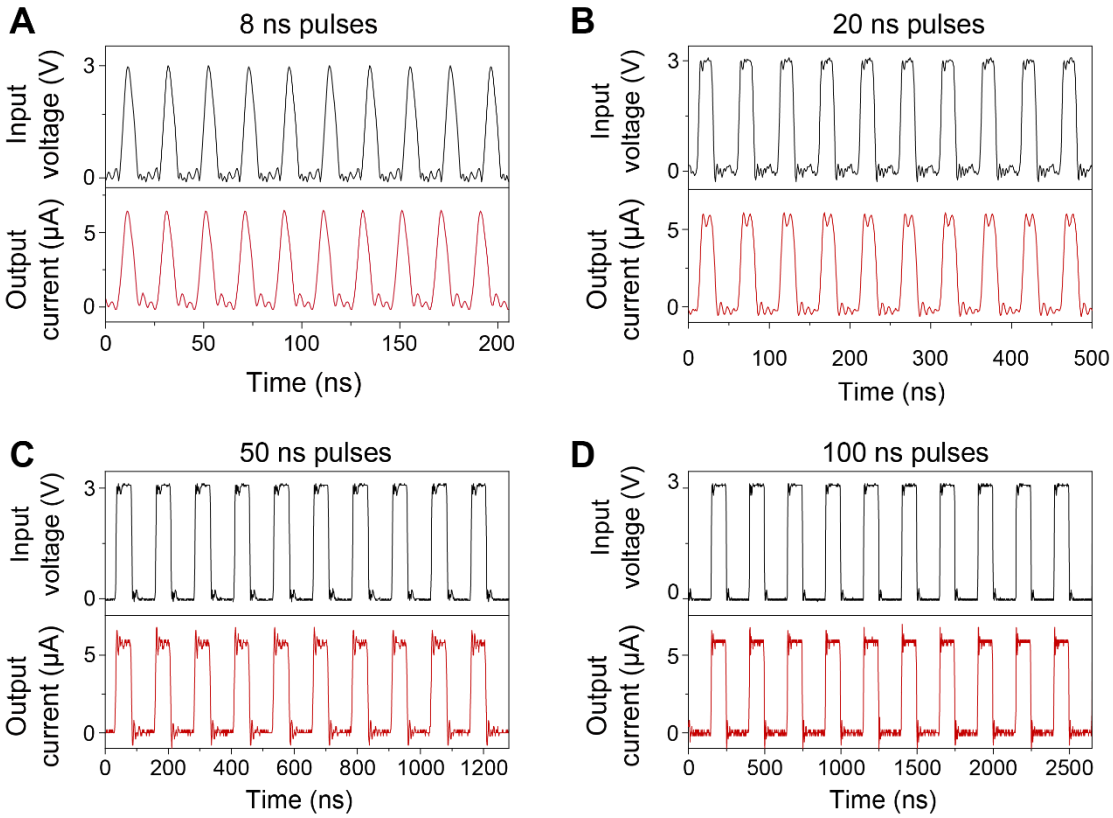


Fig. S18 Nanosecond operation speed of the synapse-mode Fe-FET for IMC. (**A**–**D**) Input voltage pulses (black) and corresponding output current responses (red) of the Fe-FET operated in synapse mode under successive V_{ds} pulses with widths of 8 ns (**A**), 20 ns (**B**), 50 ns (**C**), and 100 ns (**D**), respectively. The device maintains consistent and rapid current responses even under 8 ns pulse operation, demonstrating robust high-speed performance. Notably, 8 ns represents the resolution limit of the measurement setup rather than the intrinsic speed limit of the device, indicating that the Fe-FET is capable of operating beyond 125 MHz for IMC tasks.

Supplementary Note 2. Nonlinear activation functions enabled by reconfigurable rectification in Fe-FETs

2.1 Rationale for selecting ReLU-like activation in intermediate layers and sigmoid-like activation at the output

NAFs are essential in neural networks because they introduce nonlinearity, enabling neural networks to model complex, nonlinear separable relationships beyond linear mappings. In the system demonstrations, a ReLU-like activation is used in intermediate layers and a Sigmoid-like activation is used at the output layer. This choice is not adopted merely by convention, but follows a hardware–algorithm co-design criterion that jointly considers network behavior and hardware efficiency.

From the algorithmic perspective, intermediate layers mainly perform feature extraction and require a non-saturating activation that preserves signal dynamic range during layer-by-layer propagation. The ReLU activation provides a threshold-and-pass behavior with a linear region above threshold, which supports stable signal propagation and typically promotes sparse activations. For the output layer, the goal is probability-like readout for decision making, where a bounded saturating nonlinearity is appropriate. Although Softmax is widely used for multi-class classification, it requires global normalization across output channels, involving summation and division, which would introduce nontrivial peripheral circuitry and energy/latency overhead in an otherwise analog pipeline. In contrast, Sigmoid provides a compact node-wise mapping that can be realized directly by one device. To verify that sigmoid is an effective hardware-friendly alternative for multi-class outputs in our setting, we performed a Sigmoid-versus-Softmax comparison on CIFAR-10 under the same network architecture (fig. S19), showing closely matched accuracy (Sigmoid~84% versus Softmax ~85%).

Importantly, this mixed strategy is also well aligned with the intrinsic device physics. As detailly discussed in Supplementary Note 2.2 and 2.3, the same Fe-FET operated in a p–n configuration can be programmed into either a weakly rectifying regime that yields ReLU-like behavior or a strongly rectifying saturating regime that yields

Sigmoid-like behavior, solely by tuning the polarization-programmed junction barrier. Therefore, the network-level activation choice maps naturally onto a minimal-hardware implementation.

2.2 Polarization-programmed rectification behaviors for tunable activations

When the Fe-FET is configured in the p–n state, its output current under drain bias exhibits rectifying behavior that can be exploited as a nonlinear input–output transformation. As shown in fig. S20, the measured *I*–*V* curve can be divided into three regimes that are relevant for activation design:

- **Reverse-bias blocking** ($V_{ds} < 0$): the built-in junction potential suppresses reverse current, and the leakage is typically below 10^{-12} A, which provides an intrinsic suppression for negative inputs.
- **Nonlinear activation regime** ($0 < V_{ds} < V_T$): the forward current depends nonlinearly on V_{ds}, forming the effective nonlinear activation region.
- **Quasi-linear forward regime** ($V_{ds} > V_T$): the forward response becomes approximately linear, which is desirable when a pass-through linear region is required (e.g., ReLU-like behavior above threshold).

Here V_T is defined as a transition voltage that marks the boundary between the strongly nonlinear region and the quasi-linear forward region.

The key physical control knob for activation programming is the polarization-defined local electrostatic field in CIPS, which determines the in-plane junction barrier in the ambipolar WSe_2 channel. By programming the polarization states beneath the channel, the local junction potential and barrier profile are continuously tuned, which directly modulates rectification strength and shifts V_T (fig. S21).

As illustrated in fig. S22, weak polarization produces a shallow junction barrier, leading to a smaller V_T and an earlier onset of quasi-linear forward conduction. In contrast, strong polarization produces a higher barrier, enlarges V_T and enhances nonlinear rectification over a wider voltage range, yielding a more pronounced nonlinear response. The statistical distribution of V_T under different polarization-

programmed conditions is summarized in Fig. 4C, confirming that the activation regime is programmable and repeatable.

2.3 Hardware implementation of ReLU-like and Sigmoid-like activations

To implement ReLU-type activation, the Fe-FET is configured with a shallow junction (small V_T), allowing signals above threshold to pass linearly while suppressing negative input. For Sigmoid-like activation, a steeper junction profile (larger V_T) and a compliance current (I_{CC}) limit are applied to compress the dynamic range and emulate saturating nonlinearity. To further align the device's *I–V* curves with the mathematical forms of ideal NAFs, an offset voltage (V_{offset}) is applied to shift the *I–V* curve laterally. This translation enables the physical activation to coincide with the standard ReLU or Sigmoid functions. In this work, V_{offset} values of 0.30 V for ReLU and 0.62 V for Sigmoid were adopted (fig. S23 and S24).

To quantitatively evaluate the fidelity of Fe-FET-based NAFs, we compared the experimental *I–V* responses with ideal ReLU and Sigmoid functions using two standard metrics: Root Mean Square Error (RMSE) and Signal-to-Noise Ratio (SNR). As shown in Fig. 4 (A and B), the RMSE values were 0.005 for ReLU and 0.029 for Sigmoid, indicating excellent curve-fitting accuracy. The corresponding SNR values were ~36 dB (ReLU) and ~23 dB (Sigmoid), calculated using:

$$\mathrm{SNR(dB)} = 10 \bullet \log_{10}\left(\frac{\sum y_{\mathrm{true}}^2}{\sum\left(y_{\mathrm{exp}} - y_{\mathrm{true}}\right)^2}\right),$$

where y_{true} and y_{exp} represent the ideal and measured activation responses, respectively. The high SNR values confirm that the device can support reliable and accurate NAF operations, even in the presence of device-level variations or noise.

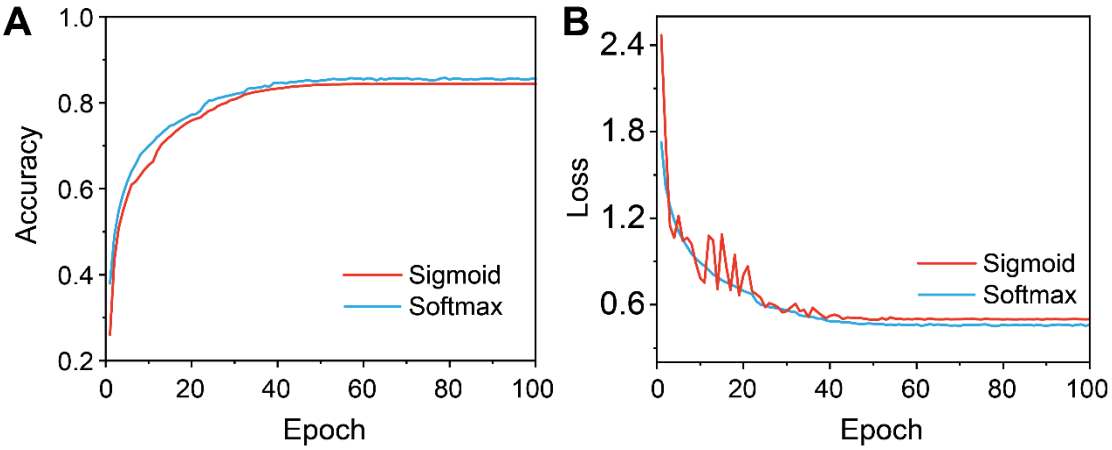


Fig. S19 Performance comparison of Sigmoid and Softmax output activations on the CIFAR-10 dataset. (**A**) Test accuracy and (**B**) training loss as a function of epoch for networks using Sigmoid (red) or Softmax (blue) at the output layer under the same architecture and training protocol. Sigmoid achieves a final accuracy of ~84%, close to the ~85% obtained with Softmax, while exhibiting similar training convergence, supporting Sigmoid as a hardware-friendly alternative for edge-efficient classification.

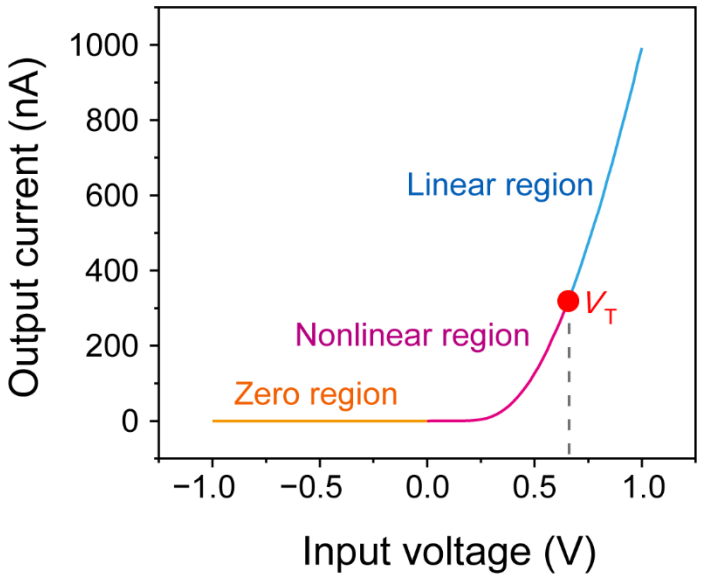


Fig. S20 Characteristic *I–V* curve of the Fe-FET in the p-n state. The rectifying *I–V* behavior of the Fe-FET can be divided into three distinct regions: a zero-current region ($V_{ds} < 0$) with suppressed reverse current, a nonlinear region ($0 < V_{ds} < V_T$) where the current exhibits exponential dependence on voltage, and a quasi-linear region ($V_{ds} > V_T$). The transition voltage V_T represents the boundary between nonlinear and linear regimes.

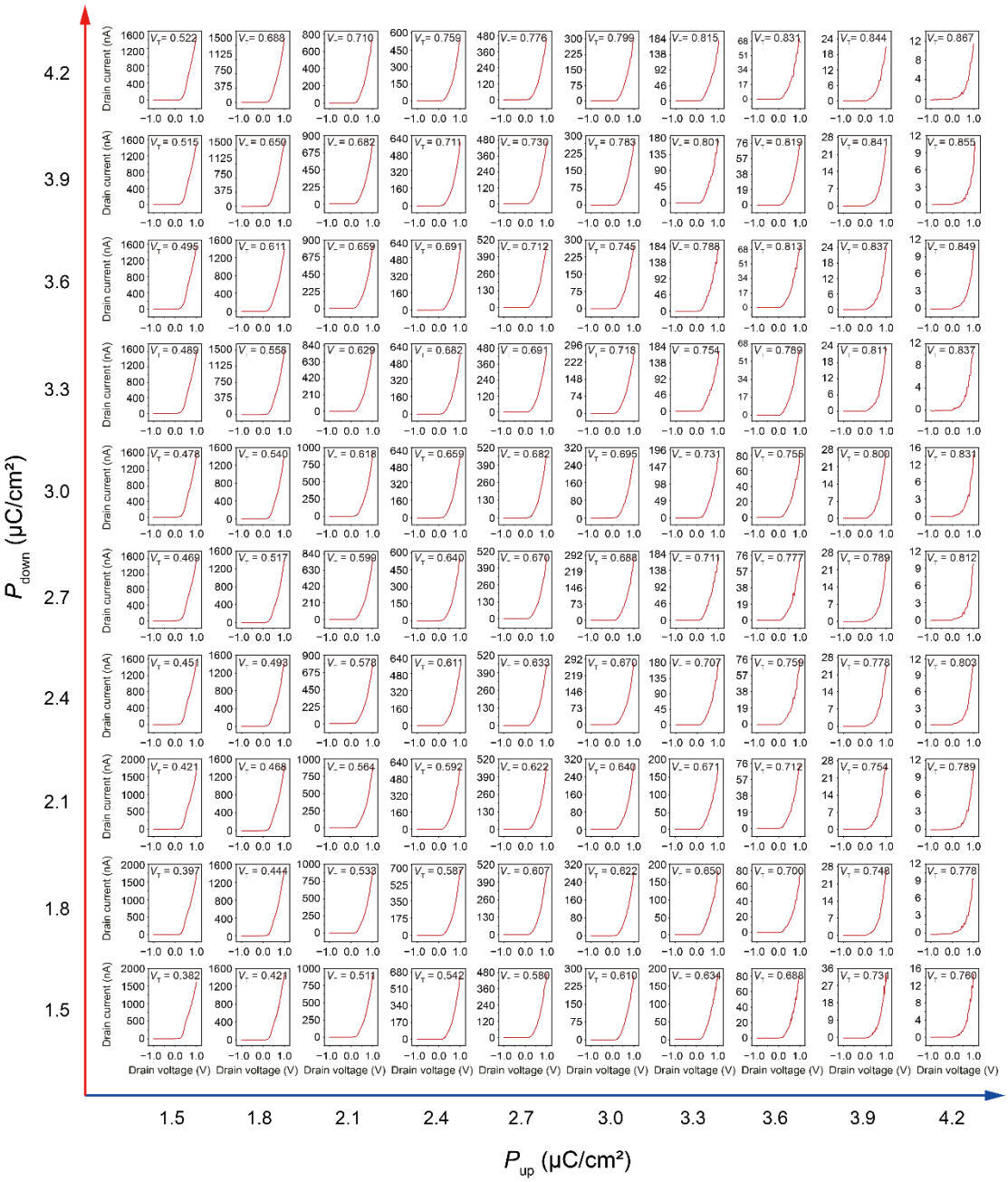


Fig. S21 *I–V* characteristics of the Fe-FET under systematic polarization modulation. Each subpanel displays the *I–V* behavior of the Fe-FET configured with different combinations of ferroelectric polarization in the CIPS layers. The horizontal axis represents the upward polarization (P_{up}) of the left CIPS region, while the vertical axis corresponds to the downward polarization (P_{down}) of the right CIPS region. Increasing either P_{up} or P_{down} enhances the local junction asymmetry, enabling systematic tuning of the rectification behavior and transition voltage V_T. This dataset reveals the device's rich configurability in supporting diverse nonlinear activation profiles.

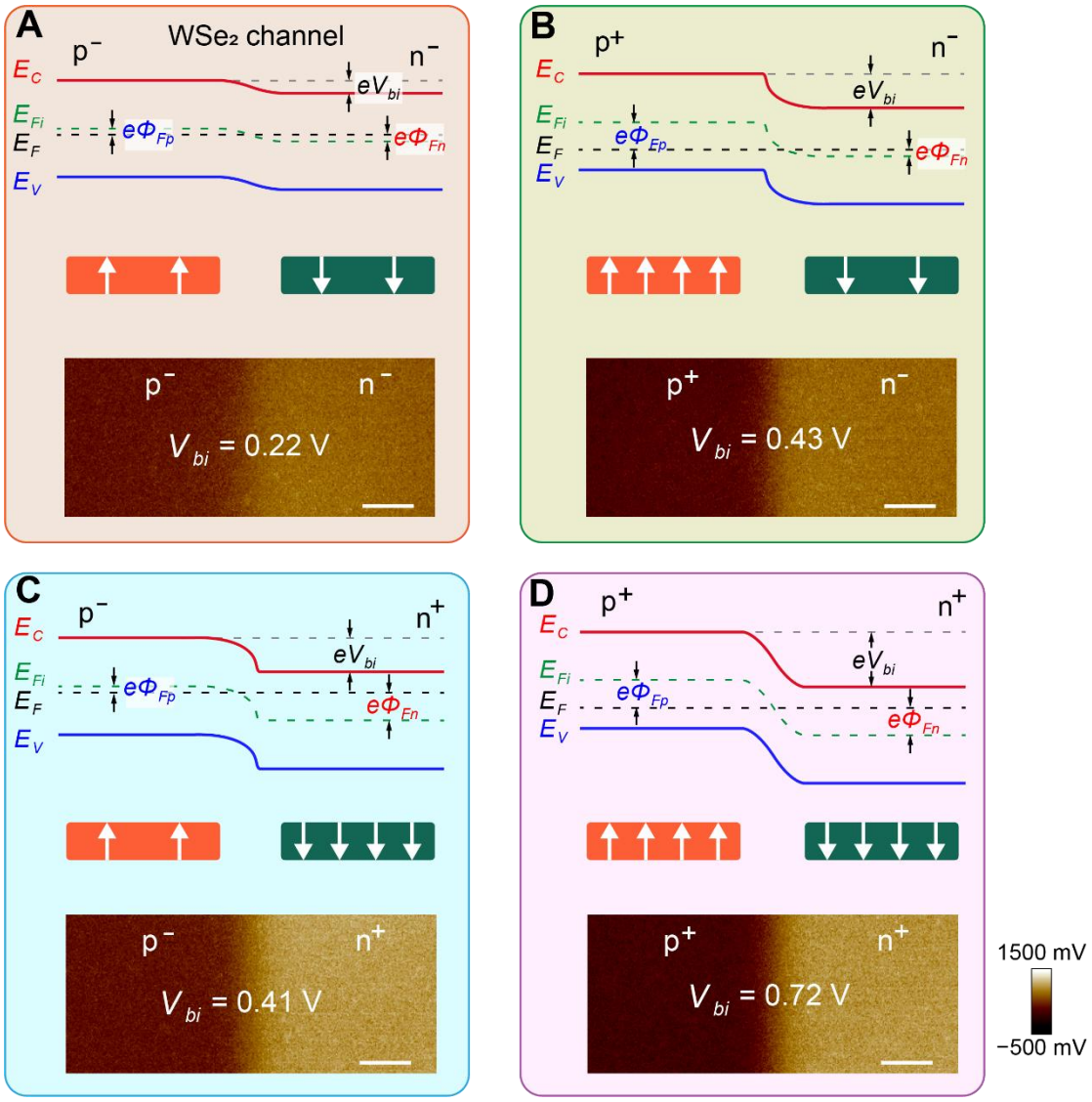
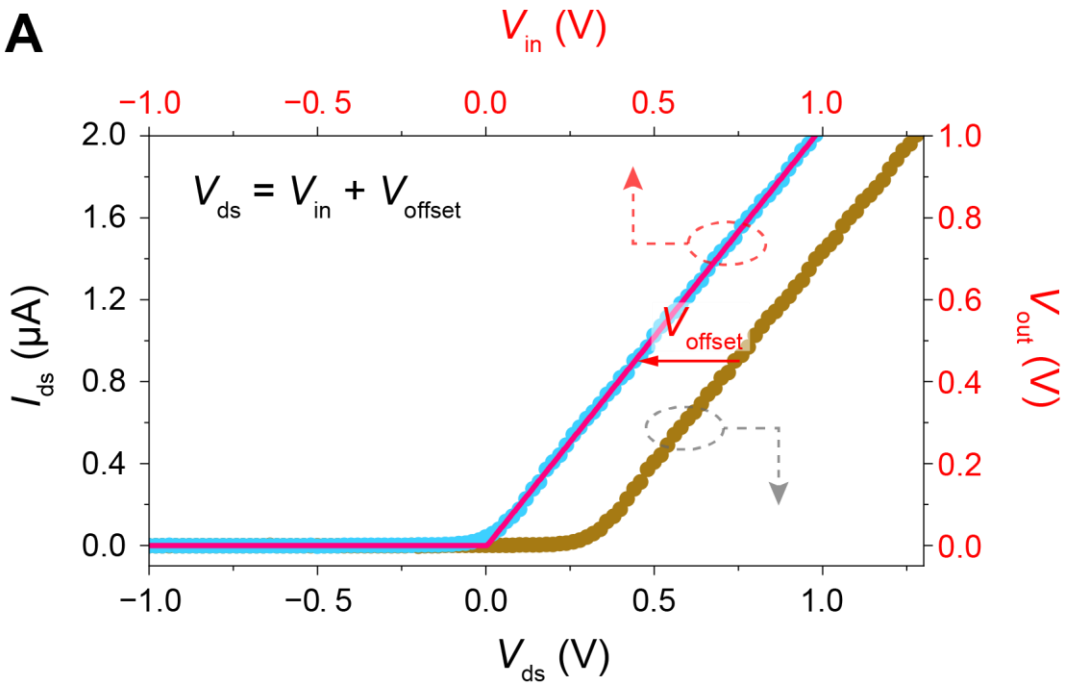
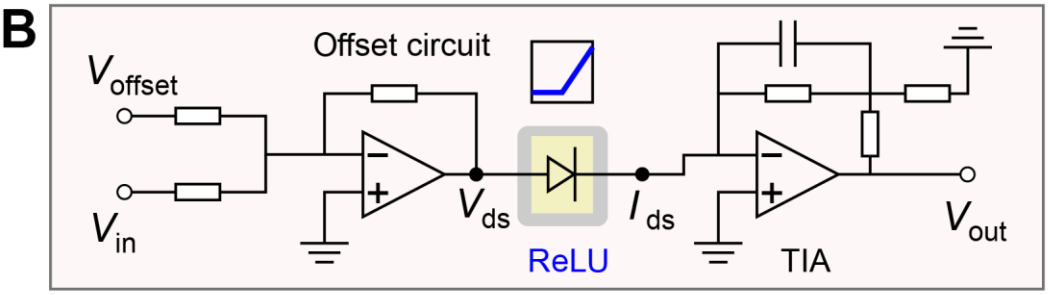


Fig. S22 Tunable built-in potential in the WSe_2 channel enabled by ferroelectric polarization. (**A**–**D**) Band alignments of the WSe_2 channel in four representative junction states: p^--n^- (**A**), p^+-n^- (**B**), p^--n^+ (**C**), and p^+-n^+ (**D**) states. Here p^-/p^+ and n^-/n^+ denote weakly and strongly doped p-type and n-type regions, respectively, induced by the polarization of the underlying CIPS layers. The local electrostatic potential—and thus the junction configuration—is precisely reconfigured by adjusting the spatial distribution and magnitude of ferroelectric polarization. The conductance band (E_C), valence band (E_V), intrinsic energy level (E_{Fi}), and Fermi level (E_F) are indicated, with ϕ_{Fp} and ϕ_{Fn} representing the electrostatic potential differences between E_F and E_{Fi} in the p-type and n-type segments. The resulting built-in potential $V_{bi} = |\phi_{Fp}| + |\phi_{Fn}|$ can be continuously tuned from ~0.2 V to ~0.7 V across different polarization combinations. Bottom panels show the corresponding KPFM maps for each configuration, validating the polarization-dependent modulation of the built-in junction. Scale bars, 500 nm.



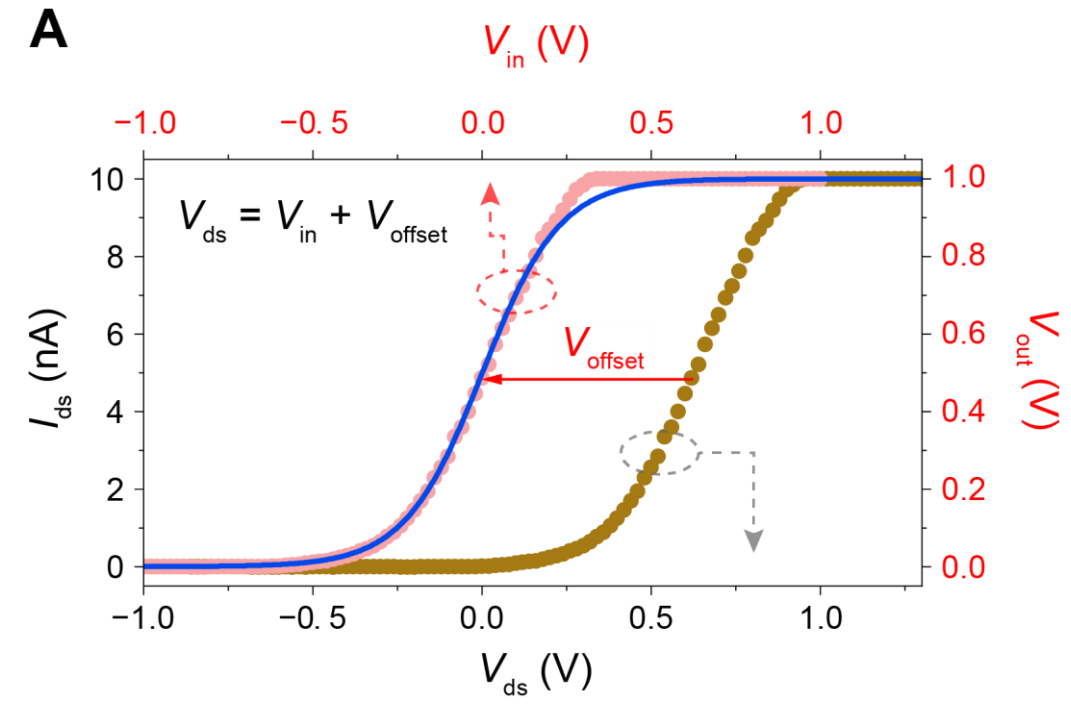


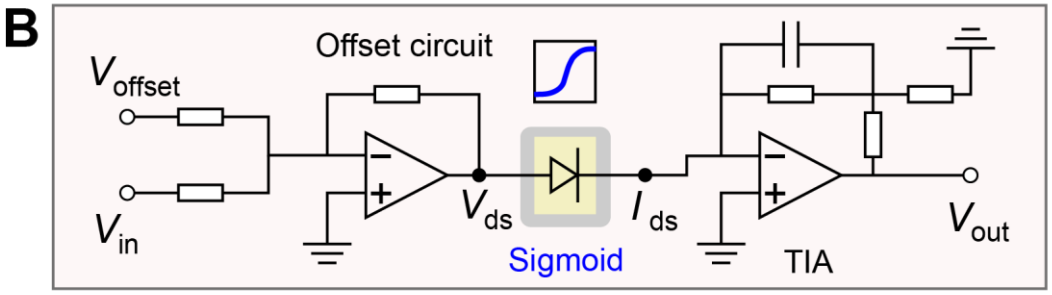
C

V_{in} (V)	−1.0	−0.5	−0.1	0.0	0.1	0.2	0.4	0.6	0.8	1.0
V_{offset}	0.3 V									
V_{ds} (V)	−0.7	−0.2	0.2	0.3	0.4	0.5	0.7	0.9	1.1	1.3
I_{ds} (μA)	0.00	0.00	0.00	0.04	0.17	0.40	0.82	1.21	1.63	2.03
V_{out} (V)	0.00	0.00	0.00	0.02	0.09	0.20	0.41	0.61	0.82	1.02

Fig. S23 Hardware implementation of ReLU activation using Fe-FETs. (**A**) Experimental *I*–*V* characteristics of the Fe-FET in ReLU configuration, showing a linear conduction regime with a small transition voltage (V_T = 0.38 V). By applying an offset voltage V_{offset}, the linear region is shifted toward V_{in} = 0 V, enabling ReLU-like behavior. The transformation follows $V_{ds} = V_{in} + V_{offset}$, allowing the device current to be expressed as $I_{ds} = a \cdot V_{in}$ after offset compensation, where a is the effective gain. (**B**) Schematic diagram of the ReLU activation circuit. The input signal V_{in} is combined

with a fixed offset voltage V_{offset} = 0.3 V to form the source-drain bias V_{ds} for the Fe-FET. The resulting drain current I_{ds} is converted to an output voltage V_{out} via a TIA, realizing hardware-based ReLU activation. (**C**) Measured input-output characteristics of the circuit in (**B**), demonstrating accurate ReLU activation. With a fixed V_{offset} = 0.3 V, negative V_{in} values are suppressed while positive inputs produce proportionally increasing I_{ds} and V_{out}, consistent with ideal ReLU function behavior.





C

V_{in} (V)	−1.0	−0.6	−0.3	−0.1	0.0	0.1	0.2	0.3	0.4	1.0
V_{offset}	0.62 V									
V_{ds} (V)	−0.38	0.02	0.32	0.52	0.62	0.72	0.82	0.92	1.02	1.62
I_{ds} (nA)	0.00	0.00	0.64	2.83	4.86	6.92	8.69	9.84	10.00	10.00
V_{out} (V)	0.00	0.00	0.06	0.28	0.49	0.69	0.87	0.98	1.00	1.00

Fig. S24 Hardware implementation of Sigmoid-type activation using Fe-FETs. (**A**) *I*–*V* characteristics the Fe-FET under Sigmoid-mode configuration. An S-shaped nonlinear conduction curve is obtained by programming a high transition voltage (V_T = 0.87 V). By applying an offset voltage V_{offset} = 0.62 V, the nonlinear activation curve is centered around V_{in} = 0 V, enabling hardware emulation of the Sigmoid function. (**B**) Schematic of the hardware Sigmoid activation circuit. The input voltage V_{in} is combined with V_{offset} to generate the source-drain bias V_{ds} for the Fe-FET. The resulting drain

current I_{ds} exhibits a compressive nonlinear response and is limited by a compliance current (I_{CC} = 10 nA) to realize saturating behavior. I_{ds} is converted to V_{out} via a TIA, achieving analog Sigmoid-type activation. (**C**) Measured input–output characteristics of the Sigmoid circuit in (**B**). With a fixed V_{offset} = 0.62 V, the Fe-FET circuit produces a nonlinear transfer function where both I_{ds} and V_{out} exhibit a saturating behavior, closely resembling the ideal Sigmoid curve.

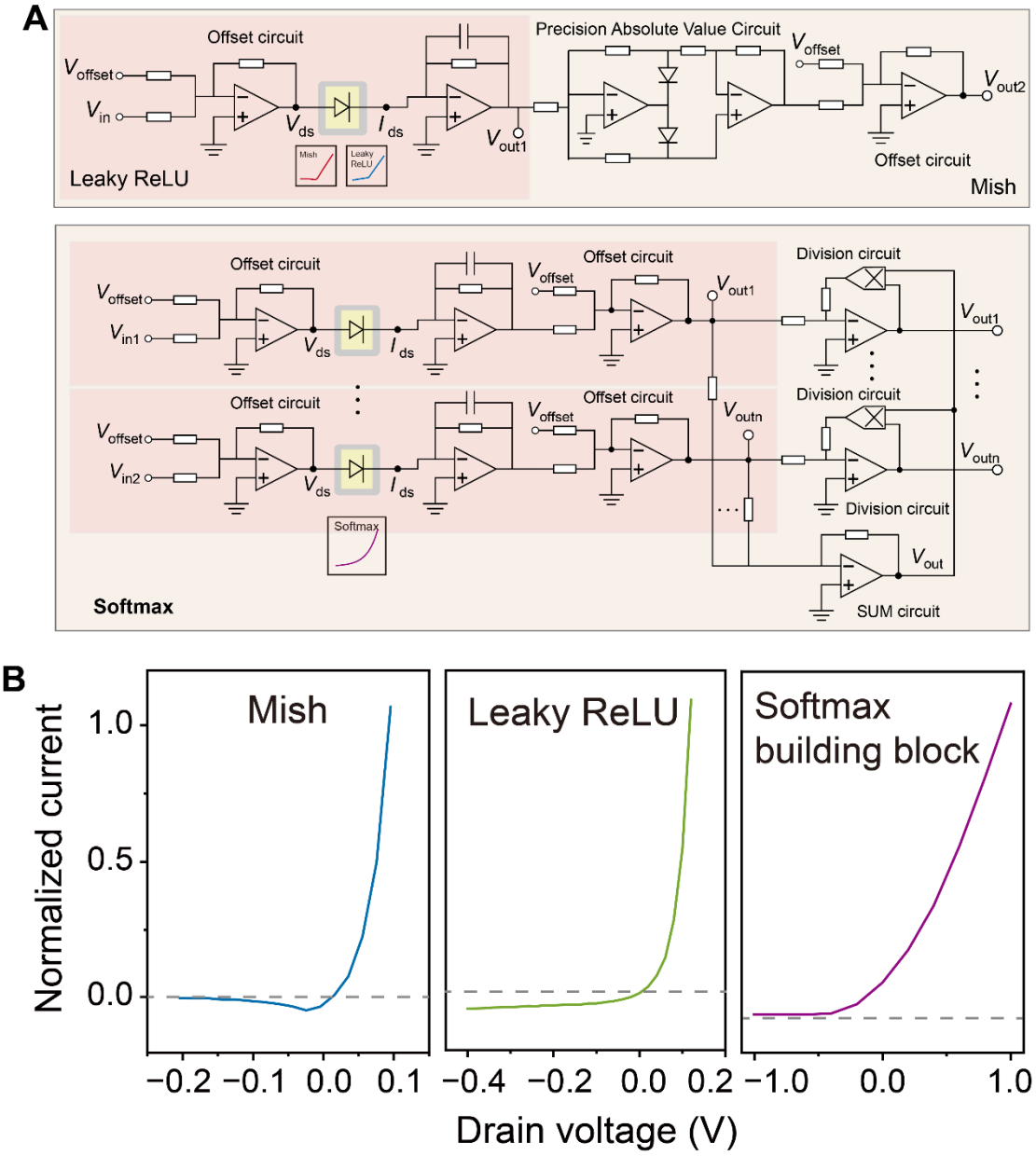


Fig. S25 Implementation of diverse complex activation functions on the Fe-FET platform. (**A**) Circuit schematics illustrating how the Fe-FET rectifying element is combined with offset and minimal auxiliary analog blocks to emulate leaky ReLU and Mish activations (top), and to form a Softmax building block that includes channel-wise preprocessing followed by summation and division for normalization (bottom). (**B**) Measured normalized output current as a function of drain voltage for the corresponding implementations, showing Mish- and leaky-ReLU–like output characteristics and the Softmax building-block response.

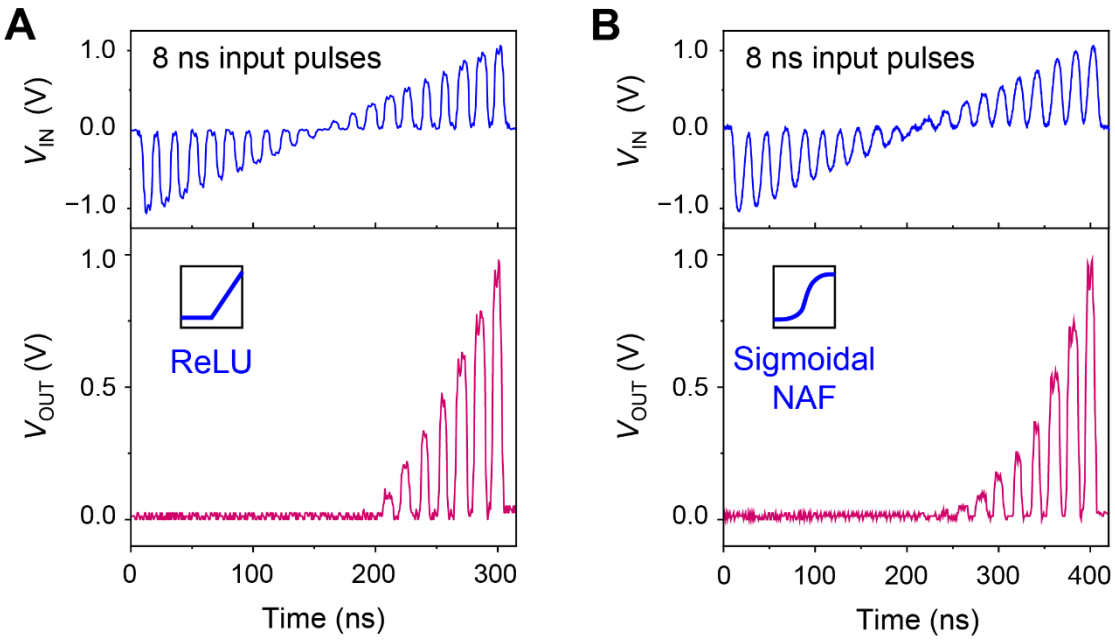


Fig. S26 Nanosecond operation speed of the Fe-FET in neuron mode for high-speed NAFs. (**A** and **B**) Dynamic response of the Fe-FET configured for NAFs under 8-ns width pulsed voltage inputs. The input waveforms (V_{IN}, top panels) sweep from –1 V to +1 V, mimicking analog neural signal variation. The output waveforms (V_{OUT}, bottom panels) exhibit ReLU-type (**A**) and Sigmoid-type (**B**) activation behaviors, demonstrating nanosecond-scale response with preserved nonlinear transformation. The results validate the Fe-FET's capability for ultrafast analog neural signal processing directly at the hardware level.

Supplementary Note 3. Uniformity of the Fe-FET array and its impact on computational accuracy

3.1 Uniformity of the morphological and spectral characterization

The performance consistency of neuromorphic device arrays critically depends on the uniformity of the underlying material system. In this work, our Fe-FET arrays are constructed using mechanically exfoliated 2D materials, which inherently provide excellent spatial homogeneity across the active region owing to their atomically flat surfaces and low defect densities.

To evaluate material homogeneity, we performed Raman mapping across the active array area. As shown in fig. S27, the characteristic peaks of CIPS and WSe_2 (e.g., δ(S-P-S) and E_{2g} modes) exhibit minimal spatial variation in both peak position and intensity, confirming high uniformity in thickness and crystallinity. The absence of significant spectral shifts also indicates low strain gradients and minimal interfacial disorder.

Furthermore, we performed AFM characterization on a representative set of 27 Fe-FET devices to evaluate surface topography. As summarized in fig. S28, the average root-mean-square (RMS) surface roughness is approximately 0.294 nm across all samples, with a standard deviation of 0.026 nm, indicating well-controlled fabrication and consistent material stacking.

These results collectively demonstrate that the Fe-FET arrays exhibit outstanding uniformity in both structural and spectral aspects. This high degree of morphological and compositional uniformity provides a robust foundation for ensuring device-to-device consistency in key electrical and optoelectronic properties. Such uniformity is essential for scalable and reliable implementation of ISC, IMC, and NAFS in hardware-level neuromorphic vision systems.

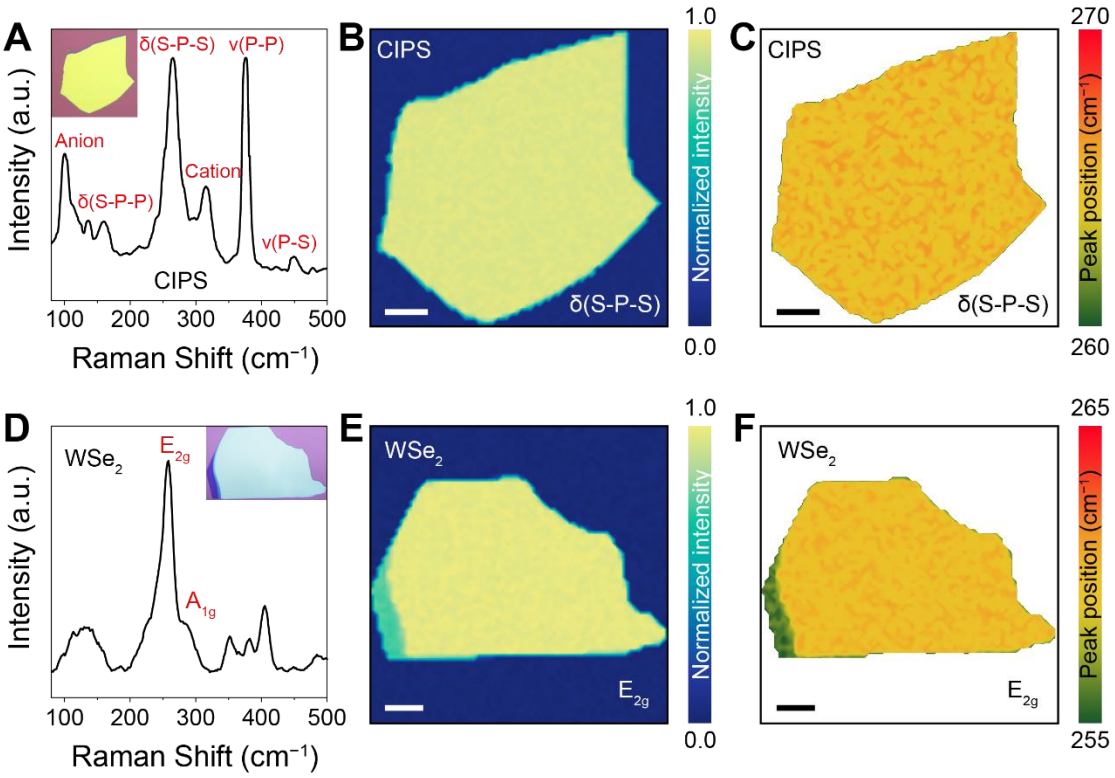


Fig. S27 Raman spectral mapping of CIPS and WSe_2 flakes. (**A**) Representative Raman spectrum of the exfoliated CIPS flake, showing characteristic vibrational modes including δ(S–P–P), δ(S–P–S), ν(P–P), and ν(P–S). (**B**) Raman intensity mapping of the δ(S–P–S) mode across the CIPS flake, revealing uniform optical contrast and signal strength. (**C**) Spatial distribution of the δ(S–P–S) peak position in the CIPS flake. The peak position remains stable near 265 cm^{-1} across the mapped region, indicating minimal strain or thickness variation. (**D**) Raman spectrum of the exfoliated WSe_2 flake, showing E_{2g} and A_{1g} vibrational modes. (**E**) Intensity mapping of the E_{2g} mode in the WSe_2 flake, confirming high signal homogeneity. (**F**) Mapping of the E_{2g} peak position across the WSe_2 flake, which remains centered around 259 cm^{-1} with minimal variation, suggesting uniform thickness and crystal quality. Scale bars, 30 μm.

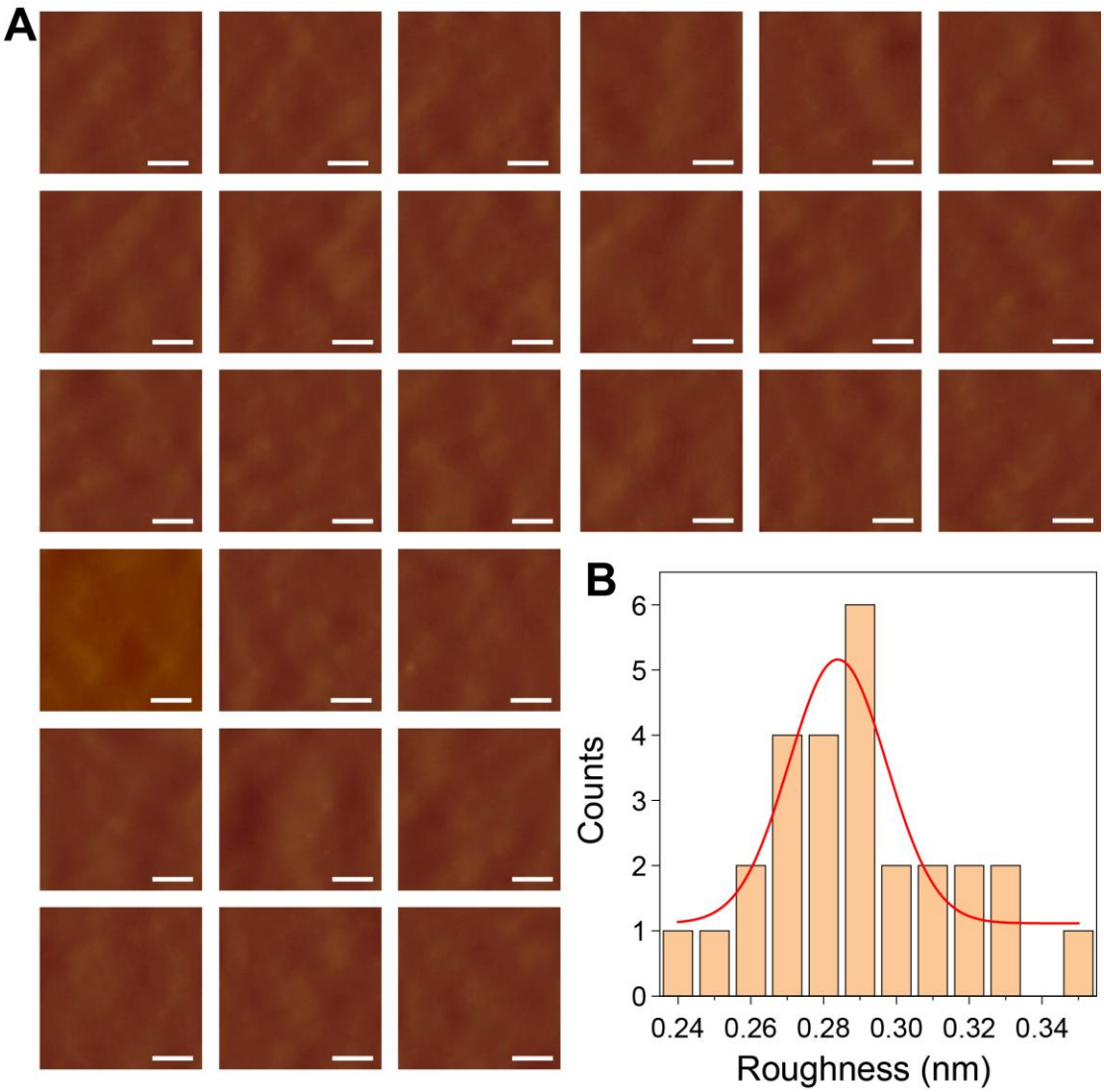


Fig. S28 Surface roughness characterization of 27 WSe_2 channels after device fabrication. (**A**) AFM images of the WSe_2 channel regions from 27 fabricated Fe-FET devices. Scale bars, 500 nm. (**B**) Statistical distribution of the root-mean-square (RMS) surface roughness across the 27 channels. The data yield an average roughness of 0.294 nm with a standard deviation of 0.026 nm, confirming high surface uniformity of the WSe_2 active layers over the entire array.

3.2 Pixel isolation and crosstalk assessment in the Fe-FET array

Reliable neuromorphic sensing and computing require that each pixel (cell) can be addressed independently without electrical leakage paths or unintended electrostatic coupling from neighboring units. Although exfoliated 2D flakes are used as starting materials, the array is not built on a laterally connected active layer. In the fabricated array, the key conductive components—including the WSe_2 channels, the MLG split control gates, and the MLG interlayers—are all patterned by femtosecond laser micromachining. This process defines each device as a physically isolated unit and removes any continuous lateral conduction path between neighboring pixels (fig. S2). As a result, the source–drain current loop is confined within an individual cell, which structurally eliminates direct electrical leakage between pixels.

The dielectric stack (hBN) is intentionally kept continuous, which is common in array fabrication because it provides uniform insulation while protecting underlying structures. Importantly, hBN is an excellent insulator with an atomically flat, dangling-bond-free surface, which suppresses interface-state – induced lateral leakage and unintended charge trapping (fig. S29A).

In this work, the ferroelectric CIPS layer is also left non-patterned. This choice does not introduce lateral crosstalk for two reasons. First, CIPS is itself a good dielectric and does not provide a lateral leakage path (fig. S29B). Second, CIPS is a layered van der Waals ferroelectric with a predominantly out-of-plane polarization axis. Owing to its intrinsic structural anisotropy, polarization switching is mainly driven by the local vertical gate field, whereas in-plane reorientation and lateral domain propagation require a substantially higher energetic cost and switching threshold (*71-73*). Consequently, lateral domain spreading is strongly suppressed under our operating conditions.

We experimentally verified this locality by directly imaging written polarization domains in CIPS. As shown in the localized PFM phase maps (fig. S30), domains written by applying a local bias exhibit sharp boundaries without observable lateral diffusion or domain-wall creep under our writing and readout conditions. Consistently,

KPFM measurements (fig. S5D and fig. S6D) show that the polarization-programmed electrostatic doping is confined to the targeted region, with no discernible potential modulation in adjacent areas. These observations confirm that the ferroelectric programming in our architecture remains spatially localized even when the CIPS layer is continuous.

To provide a direct and quantitative assessment of electrical crosstalk during active programming, we performed dynamic neighbor-coupling measurements on the array. In this test, one device was selected as the active pixel and programmed by a −7 V gate pulse, while its two nearest neighboring pixels were held under fixed bias conditions. The drain currents of all three devices were monitored simultaneously throughout the entire programming process. This measurement was repeated across all 27 devices in the 3 × 3 × 3 array, and the results are summarized in fig. S31. The programmed pixel shows the expected switching behavior, with the channel current changing rapidly from the off-state level (~10^{-13} A) to the on-state level (~10^{-6} A). In contrast, both neighboring pixels remain at the off-state baseline (~10^{-13} A) during the entire programming process, without discernible current spikes, drift, or abrupt perturbations. These results indicate robust pixel isolation over at least seven orders of magnitude under representative programming conditions.

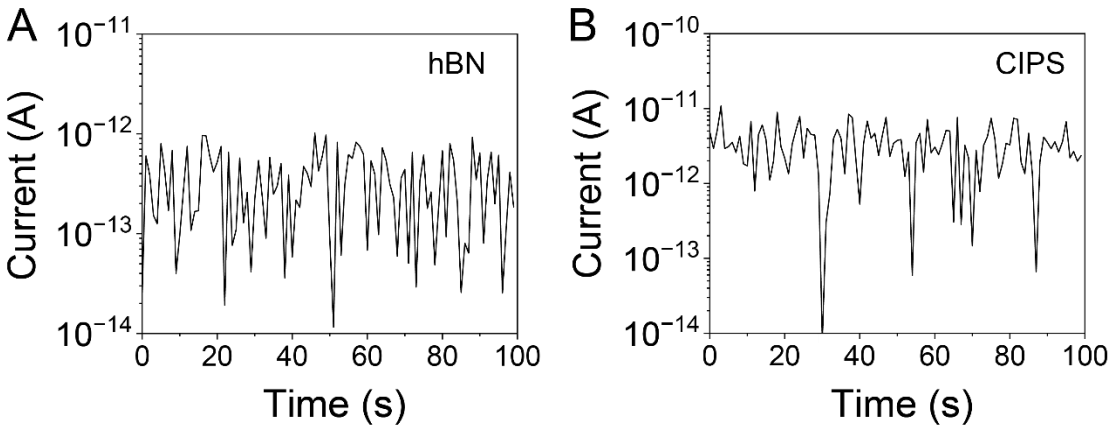


Fig. S29 Lateral leakage characteristics of non-patterned hBN and CIPS layers. (**A**, **B**) Current–voltage response measured for (**A**) the hBN layer and (**B**) for the CIPS layer under an in-plane lateral-bias configuration. Both layers exhibit ultra-low leakage currents on the order of 10^{-13}–10^{-12} A over the tested voltage range, indicating that keeping hBN and CIPS continuous does not introduce appreciable lateral leakage paths and thus does not compromise electrical isolation between adjacent devices.

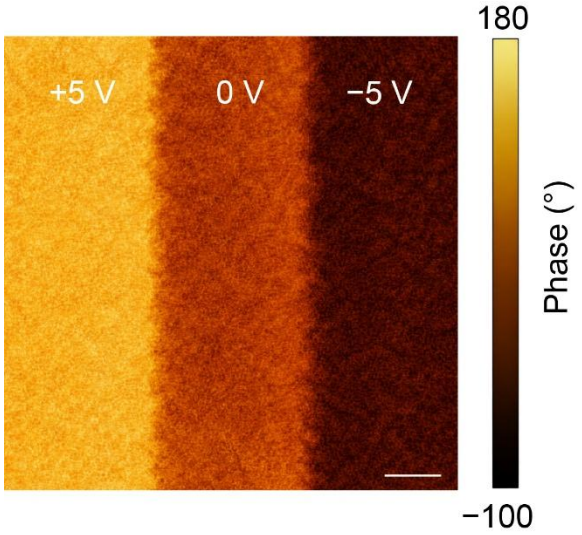


Fig. S30 PFM phase mapping of localized ferroelectric domain writing in CIPS. The PFM phase image was acquired after locally writing the CIPS surface with biases of +5 V, 0 V, and −5 V. Clear phase contrast and reversal are observed between oppositely biased regions, and the domain boundaries remain sharp with no discernible lateral diffusion, evidencing that polarization switching is confined to the electrically addressed region under local-field writing conditions. Scale bar, 1 μm.

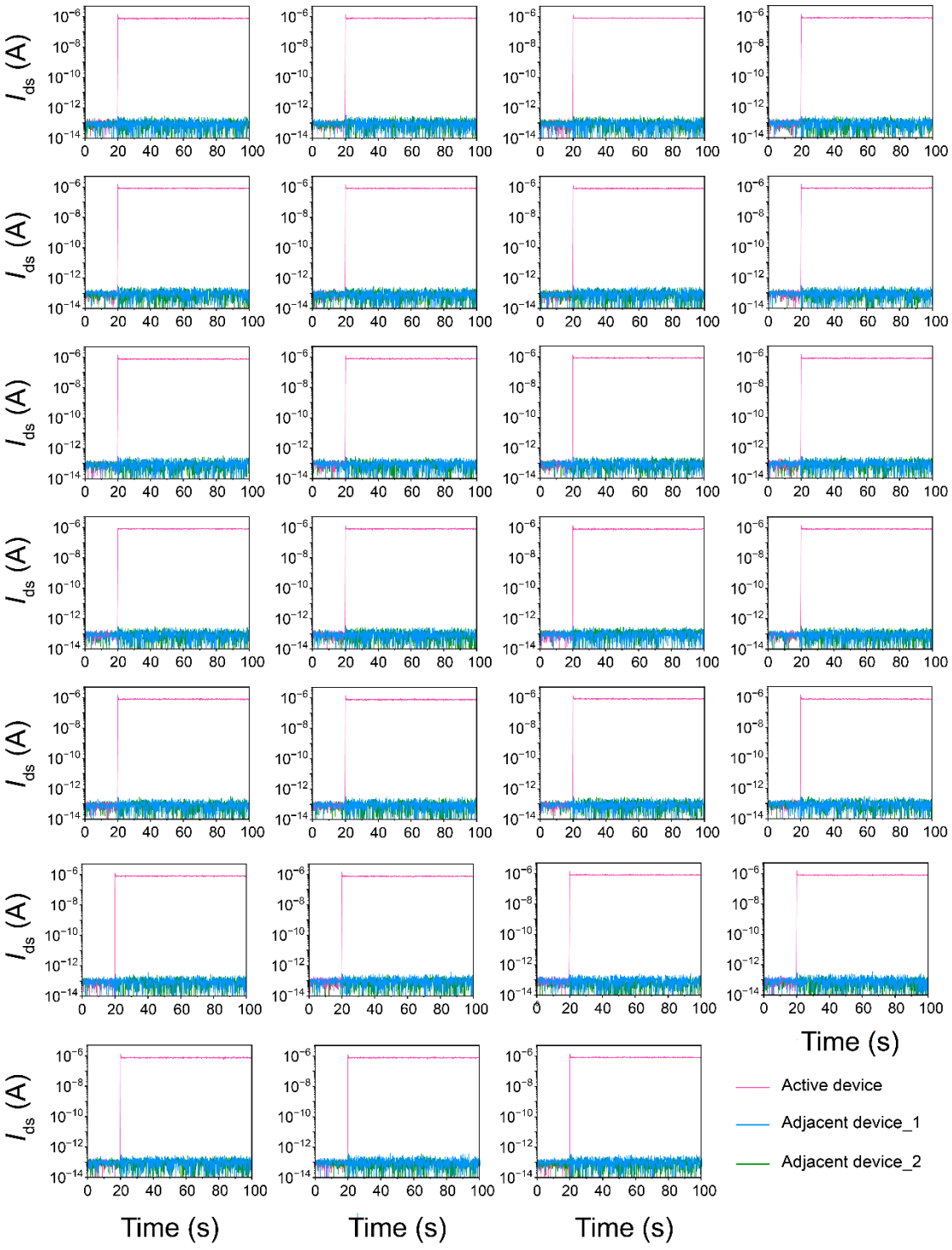


Fig. S31 Dynamic crosstalk characterization in the Fe-FET array. Drain currents I_{ds} of an actively programmed pixel (pink) and its two nearest neighboring pixels (blue and green) were recorded simultaneously during a representative programming pulse (−7 V, 1 ms). In each panel, the programmed device switches rapidly from the off-state baseline (~10^{-13} A) to the on-state level (~10^{-6} A), whereas both adjacent devices remain at the off-state baseline throughout the entire operation without discernible current spikes, drift, or perturbation. Measurements performed across all 27 devices in

the 3 × 3 × 3 array show consistent behavior, confirming negligible pixel-to-pixel crosstalk and robust electrical isolation under active programming conditions.

3.3 Performance consistency of the Fe-FET arrays for ISC, IMC, and NAF tasks

To evaluate the performance uniformity of the proposed reconfigurable Fe-FET platform under practical neuromorphic tasks, we systematically examined the response consistency of three device arrays configured for ISC, IMC, and NAFs. The uniformity of each array was quantified using device-to-device variation (DDV), defined as the normalized standard deviation across all devices under identical programming conditions. Additionally, cycle-to-cycle variation (CCV) was used to assess the stability of output signals across repeated inferences.

ISC array uniformity

For ISC evaluation, all 27 Fe-FETs in the 3 × 3 × 3 array were programmed using a closed-loop feedback protocol to achieve 33 discrete photoresponsivity (R) states over a dynamic range of ±160 mA W^{-1} (i.e., 5-bit precision). Figure S32 shows the spatial distribution of all programmed states, illustrating excellent coverage and minimal spatial deviation across the entire array. For each photoresponsivity level, the DDV was consistently below 5%, confirming high precision in analog optical weight setting.

To further examine the inference performance under practical MAC operations, combinations of input light intensity (P) and photoresponsivity (R) were projected onto the array. Figure S33 presents the resulting spatial distribution of output photocurrents for representative P−R combinations. The current outputs exhibit uniform gradients consistent with theoretical MAC expectations, validating the precision of ISC at both programming and inference stages.

Moreover, the array was tested over 10 repeated inference cycles under four representative photoresponsivity levels. As shown in fig. S34, the measured current outputs remained highly consistent across all cycles, with an average CCV of 1.5%, confirming excellent temporal stability of ISC operation.

IMC array uniformity

The IMC array consists of 3 × 9 Fe-FET devices programmed in synapse mode. Using the same pulse-tuning scheme, each device was updated to 33 conductance states ranging from 0 to 8 μS. The spatial maps in fig. S35 demonstrate narrow distribution

widths and continuous transitions across all states. The calculated DDV was below 3% at all conductance levels, reflecting excellent uniformity in electrical weight programming.

Functional testing under analog voltage input was further conducted. As shown in fig. S36, spatial distributions of output currents were recorded for a matrix of conductance–voltage (G–V) pairs. The results exhibit uniform output patterns with high signal integrity, confirming reliable MAC behavior in electrical IMC operations. The spatial current maps reveal excellent uniformity in output responses across the array, along with strong agreement with expected analog MAC results, highlighting both the computational accuracy and device-level consistency in IMC operations.

To demonstrate signal reproducibility, 10 consecutive readout cycles were performed under four representative conductance settings. As shown in fig. S37, the measured outputs exhibited minimal fluctuations, with an average CCV of 1.3%, validating the stability of IMC operation under repeated use.

NAF array uniformity

To evaluate the uniformity of nonlinear activation behavior, all 16 devices in the 4 × 4 Fe-FET array were configured into both ReLU and Sigmoid modes by tuning the ferroelectric polarization states of the underlying CIPS layers. As shown in fig. S38 and S39, all devices could be reliably configured into the target activation mode, and exhibited comparable rectifying I–V characteristics. Statistical analysis showed that the activation-threshold DDV was below 2.4% in ReLU mode and 3.3% in Sigmoid mode. This confirms that the entire array can be uniformly tuned to the same activation behavior.

We further evaluated the consistency and accuracy of activation outputs by applying a series of analog input voltages from –1 V to +1 V and recording the spatial distribution of output currents. As shown in fig. S40, the outputs across the array were highly uniform and closely matched the expected ReLU- or Sigmoid-type activation profiles. The calculated DDV of the output current was <3.5% in ReLU mode and <4.7% in

Sigmoid mode, confirming reliable nonlinear transformation and strong spatial consistency.

To assess the reproducibility of the activation behavior, four representative voltage levels were repeatedly applied across ten inference cycles. The results in fig. S41 show that the output current distributions remained stable across all repetitions for both activation modes. The average cycle-to-cycle variation (CCV) was calculated to be 1.2% for ReLU and 1.8% for Sigmoid, indicating excellent temporal stability and inference repeatability of the Fe-FET-based NAF array.

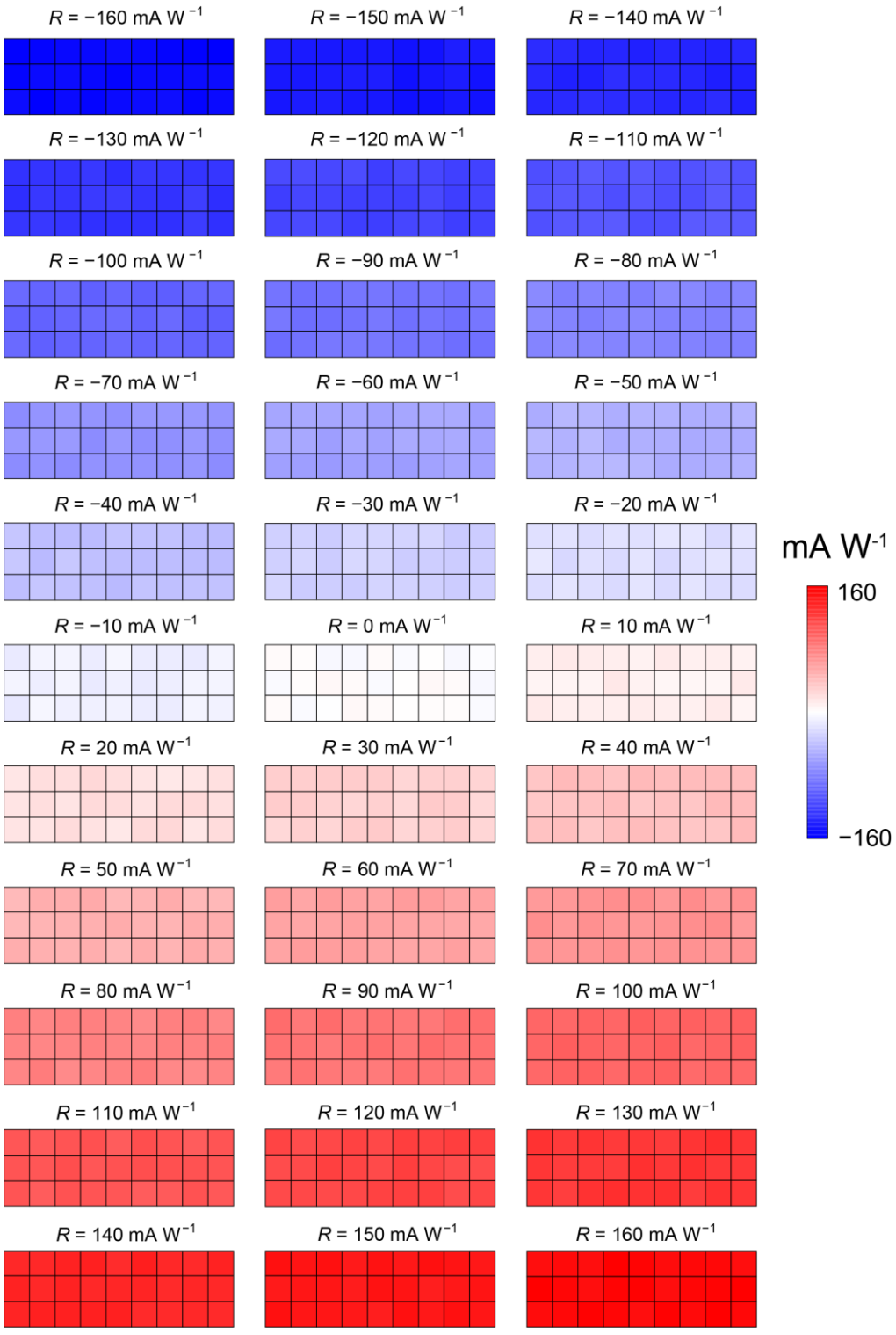


Fig. S32 Uniformity of programmable photoresponsivity states in the ISC array. Spatial distributions of photoresponsivity (R) in the 3 × 3 × 3 Fe-FET array under 33 discrete programmed states ranging from –160 to +160 mA W^{-1}. The array was programmed using closed-loop feedback pulses, achieving symmetric and continuous tuning over a wide dynamic range. The consistent color contrast across each map reflects uniform optical weight assignment with DDV < 5% at all levels.

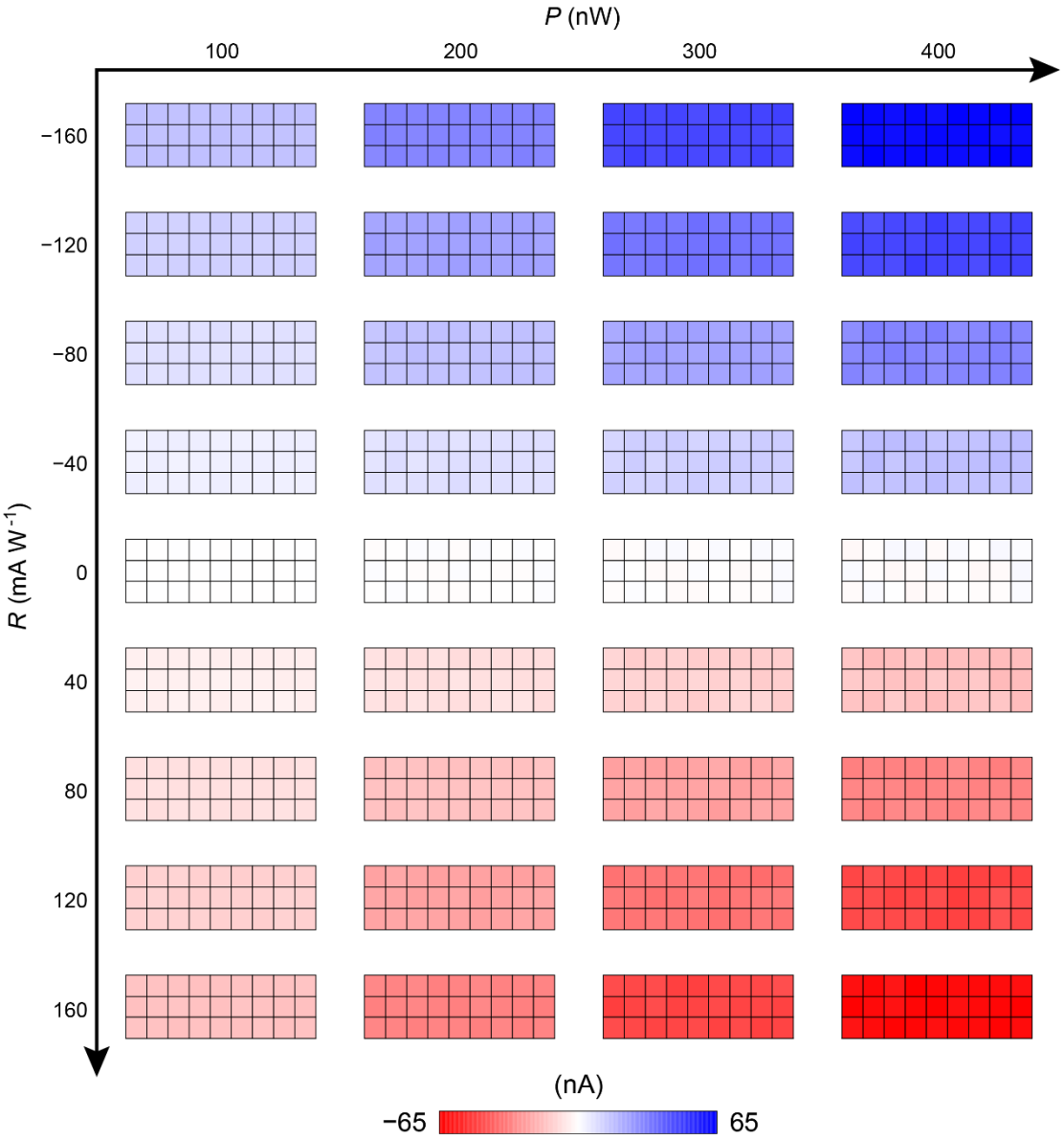


Fig. S33 ISC array output current distributions under various *P*–*R* combinations. Spatial maps of output photocurrent across the 3 × 3 × 3 ISC array under different combinations of incident light intensity (*P*) and programmed photoresponsivity (*R*). The measured currents scale linearly with both parameters and exhibit high consistency across the array. The results confirm uniform MAC behavior and low spatial variability during optical inference.

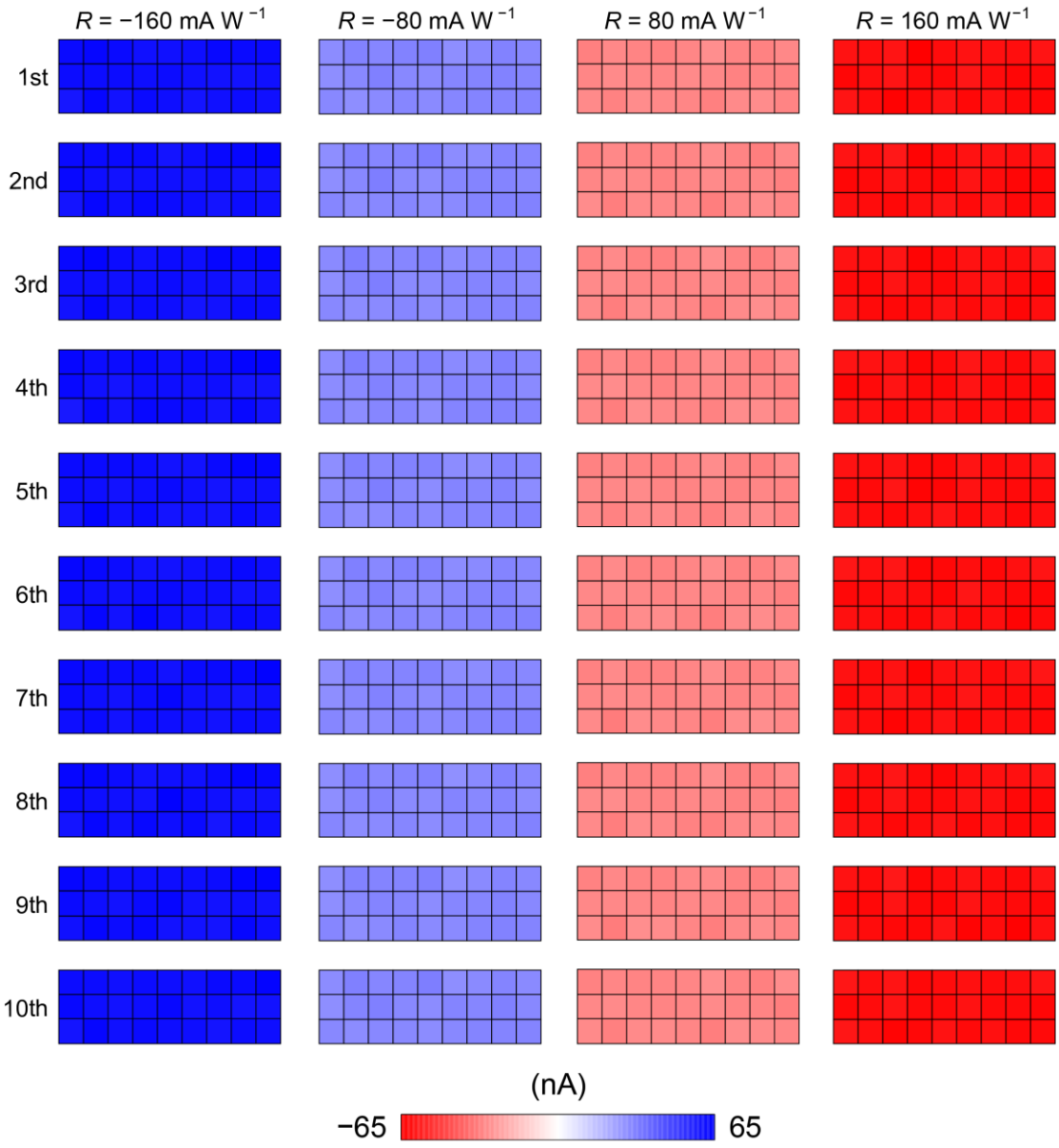


Fig. S34 Cycle-to-cycle reproducibility of ISC array under repeated optical MAC operations. Output photocurrent distributions of the 3 × 3 × 3 ISC array measured over 10 consecutive cycles under four representative photoresponsivity states (R = −160, −80, +80, and +160 mA W^{-1}). The consistent current patterns across all cycles confirm excellent reproducibility and temporal stability of the ISC module, with an average CCV of 1.5%.

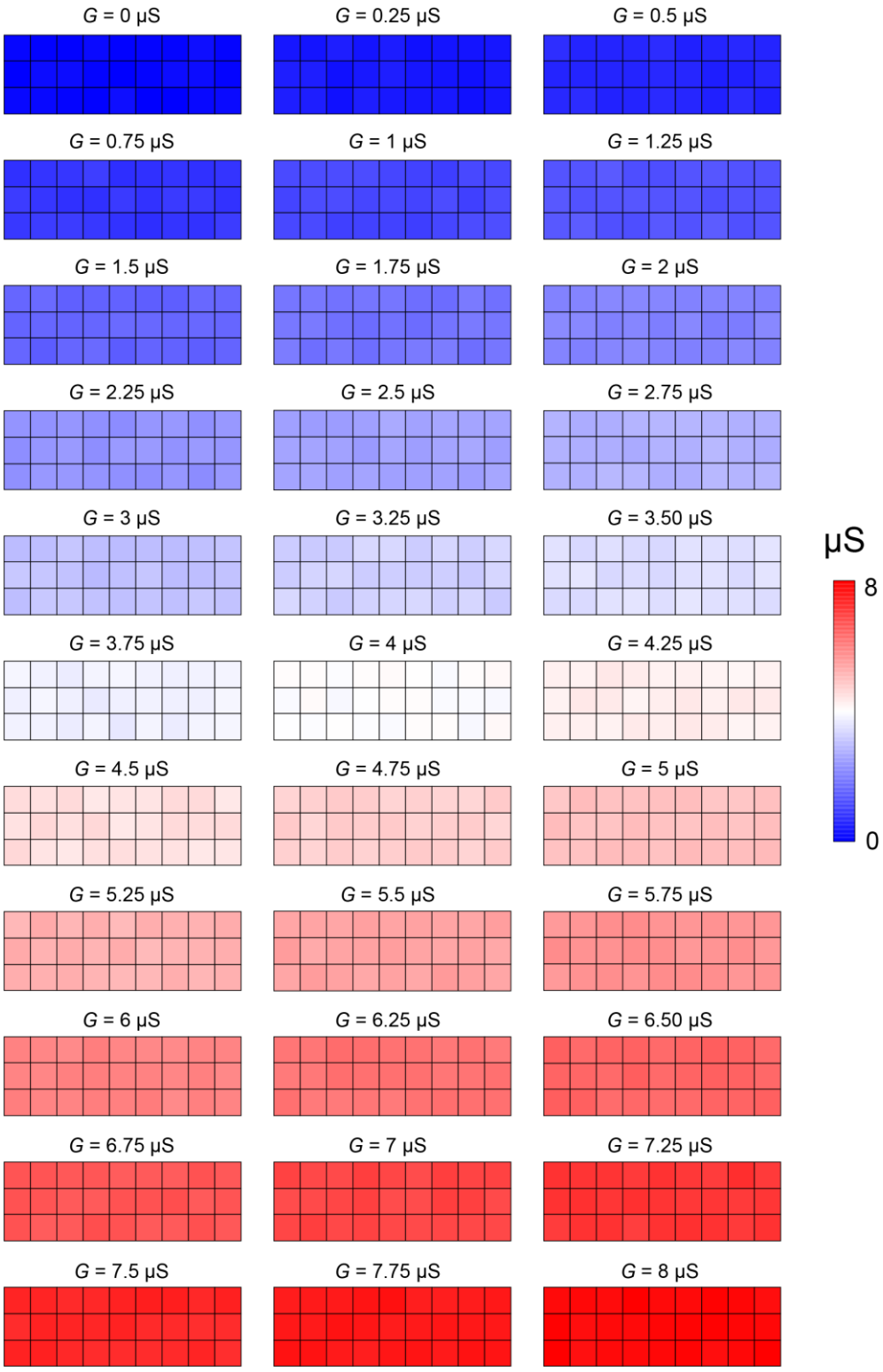


Fig. S35 Uniformity of programmable conductance states in the IMC array. Spatial distributions of conductance (G) in the 3 × 9 Fe-FET array for 33 programmed states from 0 to 8 μS. Each device was tuned using closed-loop feedback pulses. The smooth and monotonic color transitions across the array indicate high programming precision and uniformity, with DDV values consistently below 3% across the full conductance range.

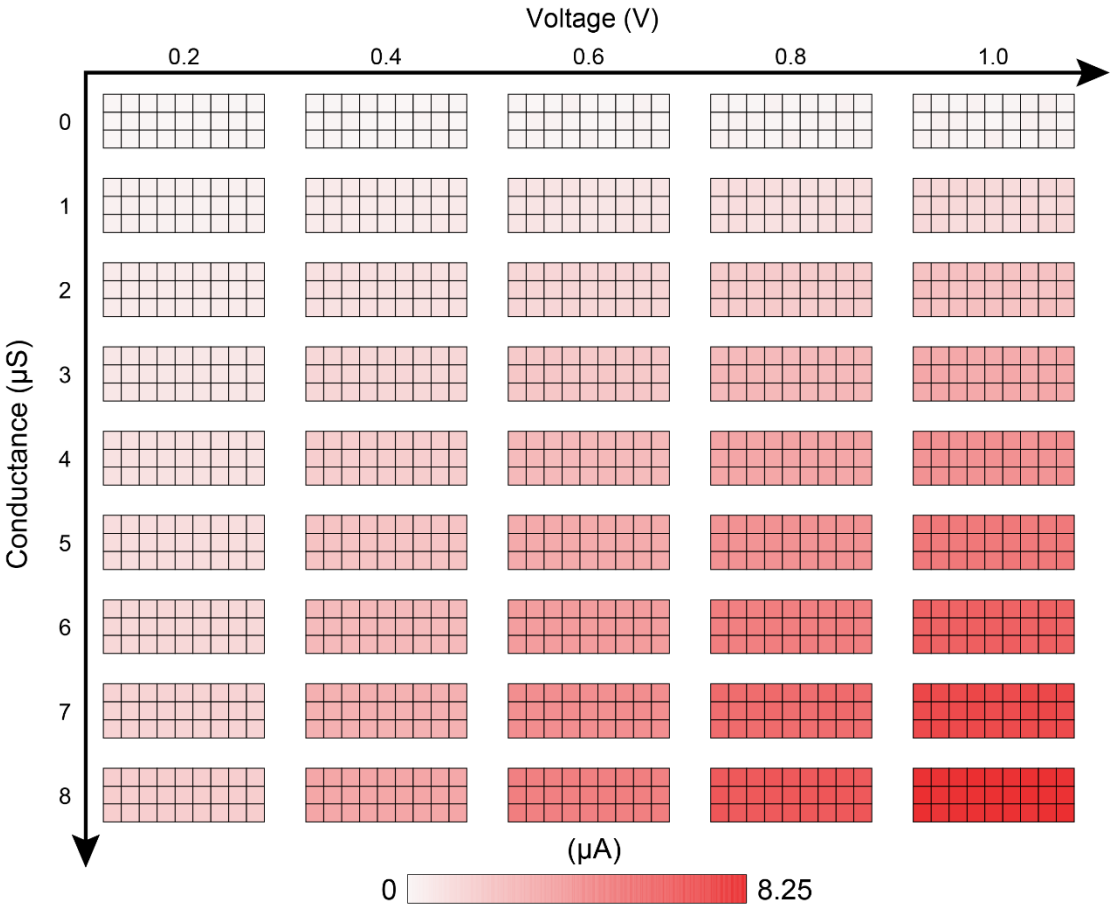


Fig. S36 Output current distributions of the IMC array under various *G*–*V* combinations. Spatial distributions of output current across the 3 × 9 IMC array for selected combinations of programmed conductance (*G*) and applied input voltage (*V*). The results exhibit excellent signal uniformity and close agreement with theoretical analog multiplication, validating the consistency and accuracy of in-memory MAC operations across the array.

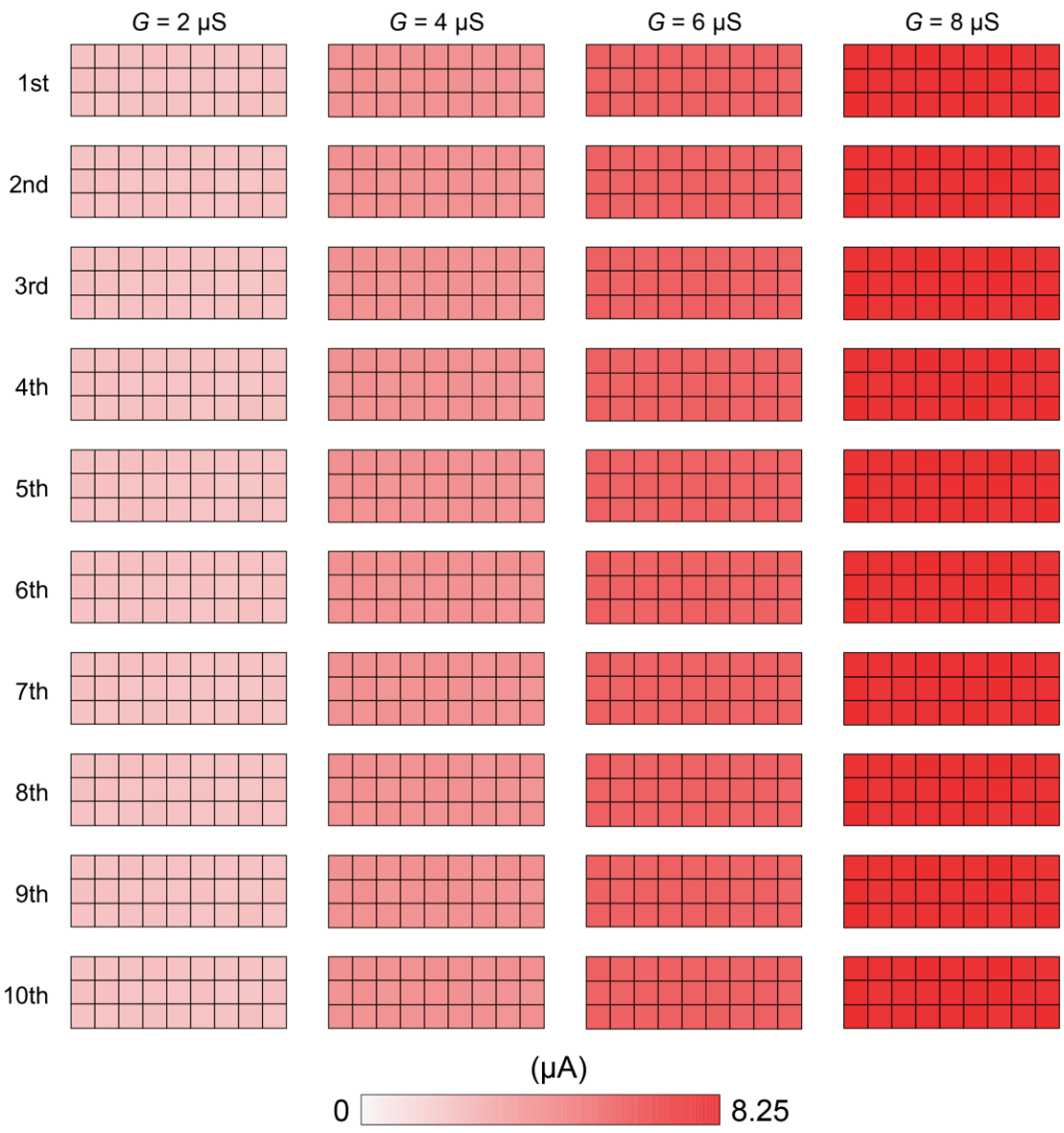


Fig. S37 Cycle-to-cycle reproducibility of IMC array under repeated electrical MAC operations. Output current distributions of the 3 × 9 IMC array recorded over 10 consecutive cycles for four representative conductance states (G = 2, 4, 6, and 8 μS). The results demonstrate high stability of analog MAC response under electrical input conditions, with an average CCV of 1.3%.

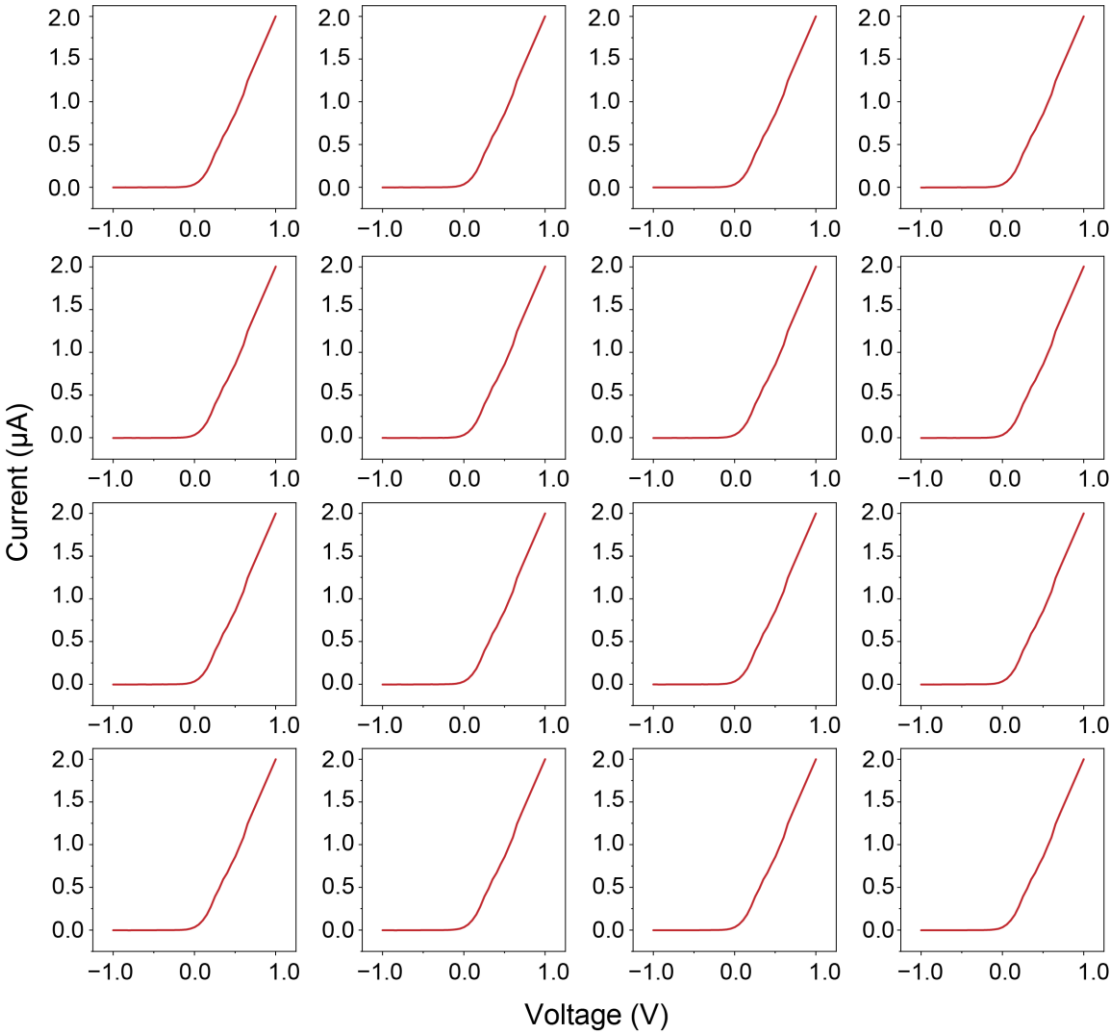


Fig. S38 Circuit-level verification of ReLU-type activation uniformity in a 4 × 4 Fe-FET array. Output characteristics measured from all 16 cells in the 4 × 4 activation array under the ReLU configuration. Each device exhibits a consistent rectifying turn-on with a quasi-linear pass region for positive bias and suppressed output near zero/negative bias, yielding closely matched transition voltages V_T (DDV < 2.4%) and comparable slopes. The directly measured circuit outputs confirm device-to-device uniformity and reliable array-level operation in the ReLU activation regime.

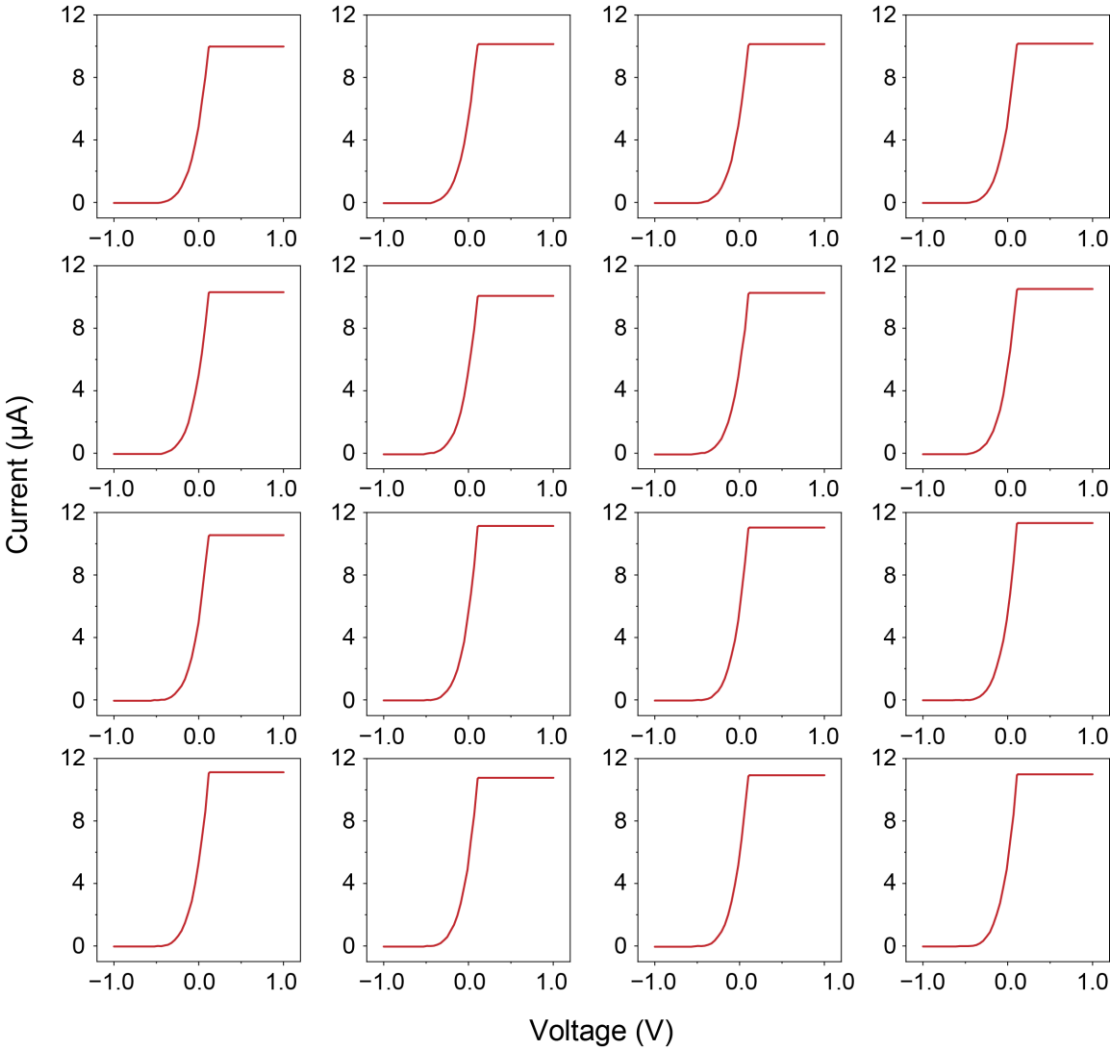


Fig. S39 Circuit-level verification of sigmoid-type activation uniformity in a 4 × 4 Fe-FET array. Output characteristics measured from all 16 cells in the 4 × 4 activation array under the sigmoid configuration. The devices show highly consistent S-shaped input–output curves, with closely matched transition voltages V_T (DDV < 3.3%) and similar saturation behavior across the array.

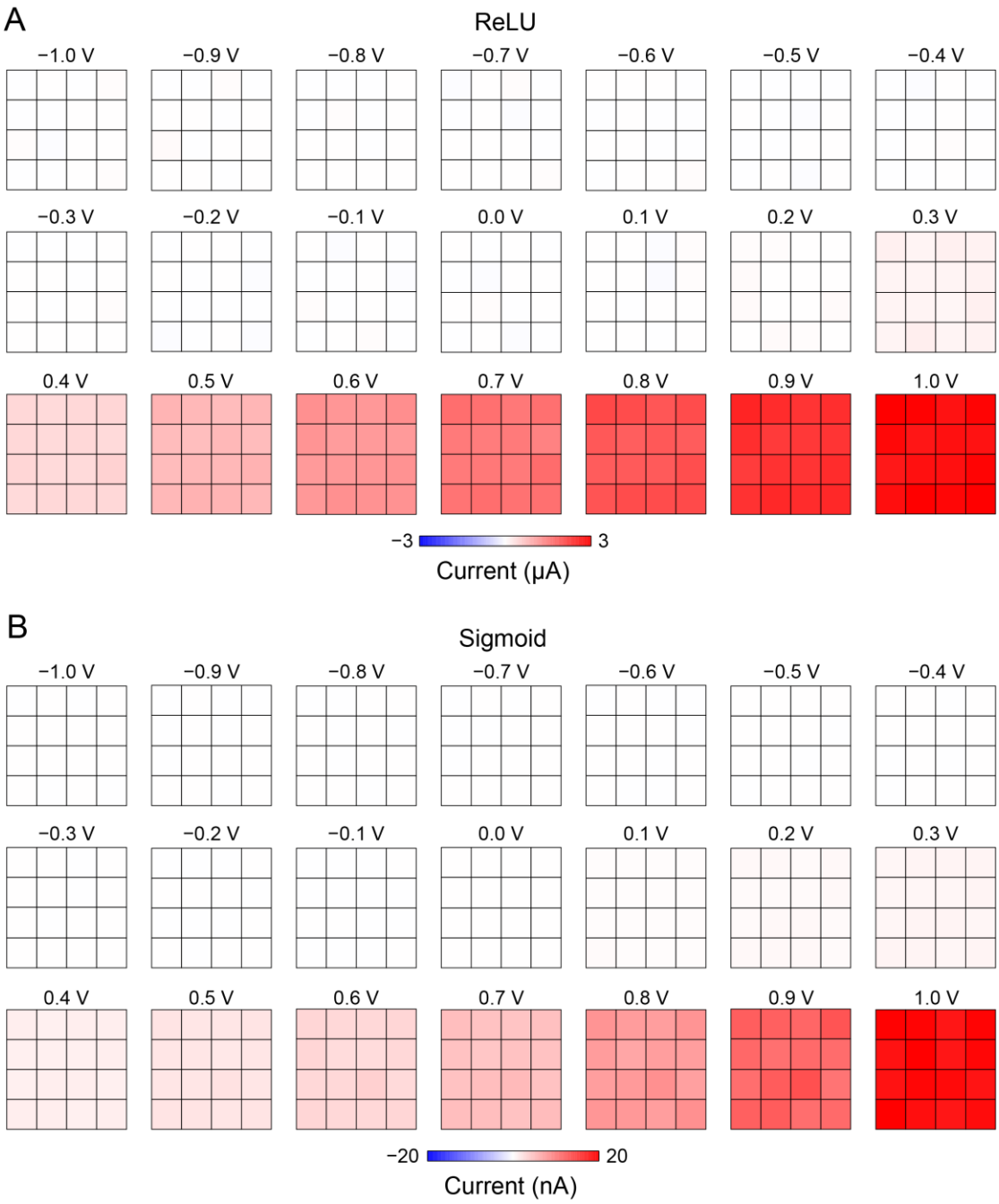


Fig. S40 Spatial output uniformity of the NAF array in ReLU and Sigmoid modes. Spatial distributions of output current from the 4 × 4 Fe-FET activation array under analog input voltages ranging from –1 V to +1 V. Panels show responses in ReLU (**A**) and Sigmoid (**B**) configurations. The output signals exhibit high uniformity and match expected activation profiles with DDV of 3.5% for ReLU and 4.7% for Sigmoid, confirming consistent nonlinear transformations across the array.

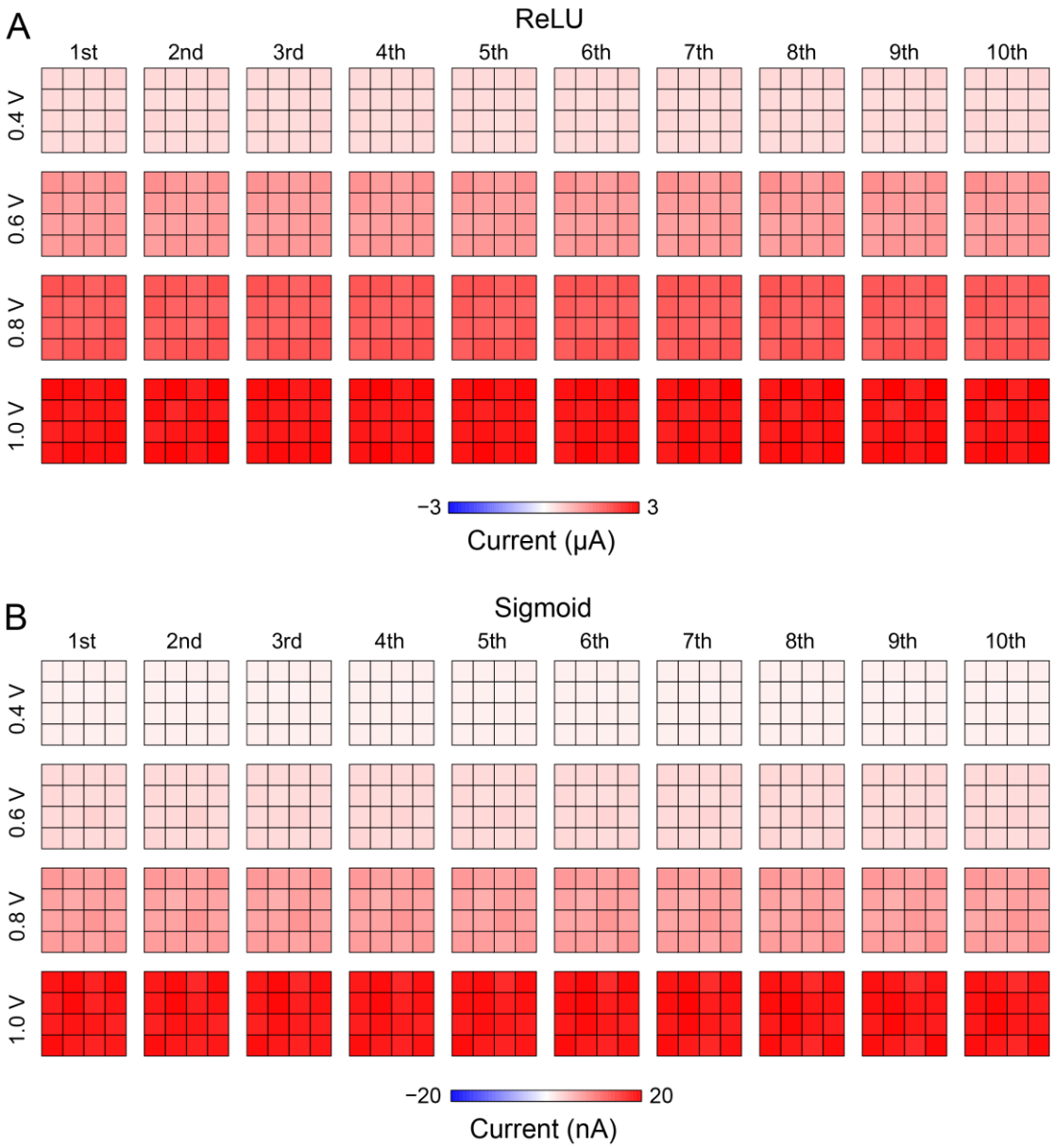


Fig. S41 Cycle-to-cycle reproducibility of 4 × 4 Fe-FET activation array under repeated inference. Output current distributions of the 4 × 4 NAF array measured over ten consecutive cycles under four representative input voltages for ReLU (**A**) and Sigmoid (**B**) activation modes. The outputs remain stable across all cycles, with average CCV of 1.2% and 1.8%, respectively, confirming the temporal reliability and operational robustness of the Fe-FET–based NAF implementation.

3.4 Temperature stability of the Fe-FET array

CIPS is an ion-assisted, layered van der Waals ferroelectric in which Cu-related dipole configurations govern the polarization state. Since polarization-controlled local electrostatics determines the junction-barrier tuning and thus the behaviors of the Fe-FET, evaluating the thermal stability of both the ferroelectric layer and the Fe-FET is essential for practical neuromorphic operation.

Temperature dependence of ferroelectric switching in CIPS

The intrinsic thermal robustness of CIPS was examined by measuring polarization–voltage (*P–V*) hysteresis loops at different temperatures and extracting the remanent polarization P_r (fig. S42). As temperature increases from 298 K to 310 K, P_r shows a moderate decrease accompanied by a slight narrowing of the hysteresis loop, consistent with thermally enhanced fluctuations that weaken the ferroelectric order parameter in ion-assisted ferroelectrics. Importantly, within this temperature window, the remaining P_r stays sufficiently large to sustain the electrostatic modulation required for programming the WSe_2 channel band profile and junction barrier, indicating that the functional polarization margin is preserved under moderate thermal variation.

Array-level electrical evolution with temperature

To assess device-level and array-level stability, variable-temperature electrical measurements were performed on all 27 devices in the 3 × 3 × 3 array (fig. S43). Below 310 K, the p–p ON-state current remains near the 10^{-6} A level with a narrow distribution, while the n–p OFF-state current increases mildly with temperature. As the temperature approaches the Curie-region window (315–320 K), the ON-state current decreases, which correlates with the thermal attenuation of ferroelectric polarization.

This behavior can be understood from the device operating mechanism: the programmable in-plane junction in the WSe_2 channel is defined by polarization-induced local electrostatic doping from the CIPS layer. As the temperature approaches the Curie temperature (*74, 75*) (~315–320 K), the reduced polarization strength leads to weakened electrostatic doping. Consequently, in the ON state (p–p configuration), the decreased hole concentration reduces channel conductance, while in the OFF state (n–

p configuration), the reduced doping lowers the junction barrier height, resulting in increased reverse current. These combined effects lead to a degradation of the ON/OFF ratio near the Curie temperature.

Notably, the temperature-dependent trends and current distributions are highly consistent across all 27 devices, suggesting uniform and predictable thermal response rather than sporadic device-specific instabilities.

Retention and drift characteristics of the Fe-FET under thermal stress

Long-term stability under thermal stress was evaluated by comparing nonvolatile retention at 298 K and 310 K (fig. S44). Both high- and low-conductance states remain stable over 10^4 s at 310 K, with no discernible resistance drift or state degradation. This behavior indicates that, under the explored operating conditions, Cu-ion-related polarization states are sufficiently constrained to maintain reliable weight retention, supporting stable neuromorphic inference without refresh.

Discussion on thermal limitation and mitigation strategies

It should be noted that the thermal limitation discussed above is primarily associated with the high-temperature regime near the Curie temperature of CIPS. In contrast, at lower temperatures, ferroelectric polarization in CIPS is generally more stable due to suppressed ionic motion, and previous studies have demonstrated that remanent polarization can persist down to 100 K, and gradually disappears only at much lower temperatures (*74, 75*) (<50 K). In addition, the ambipolar transport characteristics of the WSe_2 channel are known to remain robust over a wide temperature range (*76*). Therefore, low-temperature operation is not expected to impose a fundamental limitation on device functionality, although systematic low-temperature characterization is beyond the scope of the present study.

The observed performance degradation above ~310 K thus represents an intrinsic limitation associated with the proximity to the Curie temperature of CIPS. Therefore, while the present device exhibits stable operation within a practically relevant temperature range around room temperature, extending the operating temperature window is important for broader applications.

Several strategies may be adopted to improve the thermal robustness. At the material level, enhancing the crystalline quality of CIPS—particularly by reducing Cu vacancies, sulfur vacancies, and uncontrolled interstitial Cu ions—can suppress temperature-activated ionic migration and mitigate ferroelectric degradation (*75*). At the device level, optimizing the MFMIS structure to improve depolarization field screening and interface cleanliness can stabilize the polarization-induced local electric field, thereby enhancing the thermal stability of the programmable junction barrier. In addition, device encapsulation and thermal management can help suppress environmental perturbations and local heat accumulation during operation.

For applications requiring elevated-temperature operation, a longer-term strategy is to retain the reconfigurable device concept while employing ferroelectric materials with higher Curie temperatures, such as HfO_2-based ferroelectrics (*77*) or $LiNbO_3$ (*78*) which have demonstrated improved thermal robustness in prior studies.

All these results demonstrate that the CIPS-programmed Fe-FET platform retains robust programmability, uniform thermal response across the array, and low-drift nonvolatility within the practical operating temperature range relevant to neuromorphic hardware.

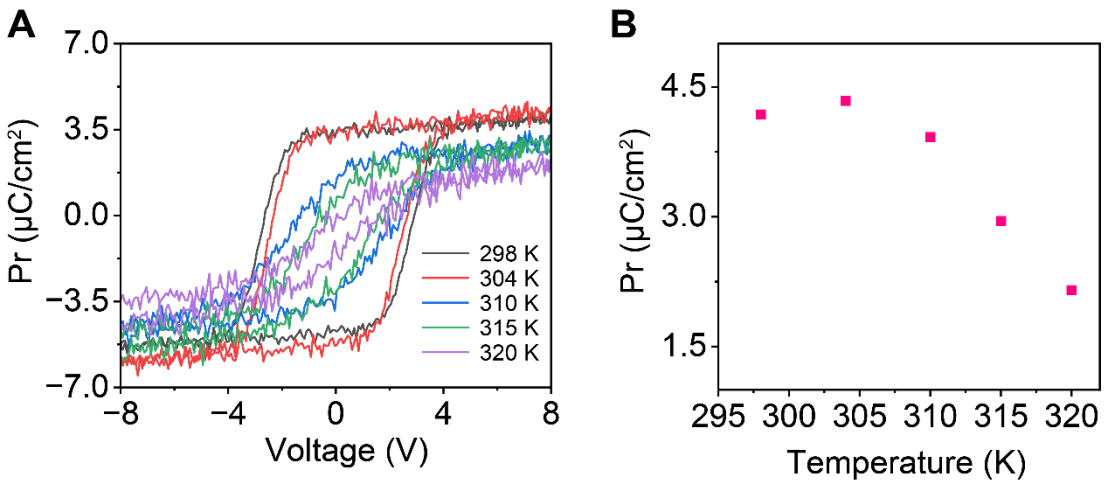


Fig. S42 Temperature-dependent ferroelectric characteristics of CIPS. (**A**) Polarization–voltage (*P*–*V*) hysteresis loops measured at 298–320 K. (**B**) Extracted remanent polarization P_r as a function of temperature. With increasing temperature, the hysteresis loop gradually narrows and P_r decreases moderately, yet the remaining polarization remains sufficient to provide effective electrostatic modulation for junction-barrier programming in the Fe-FET devices.

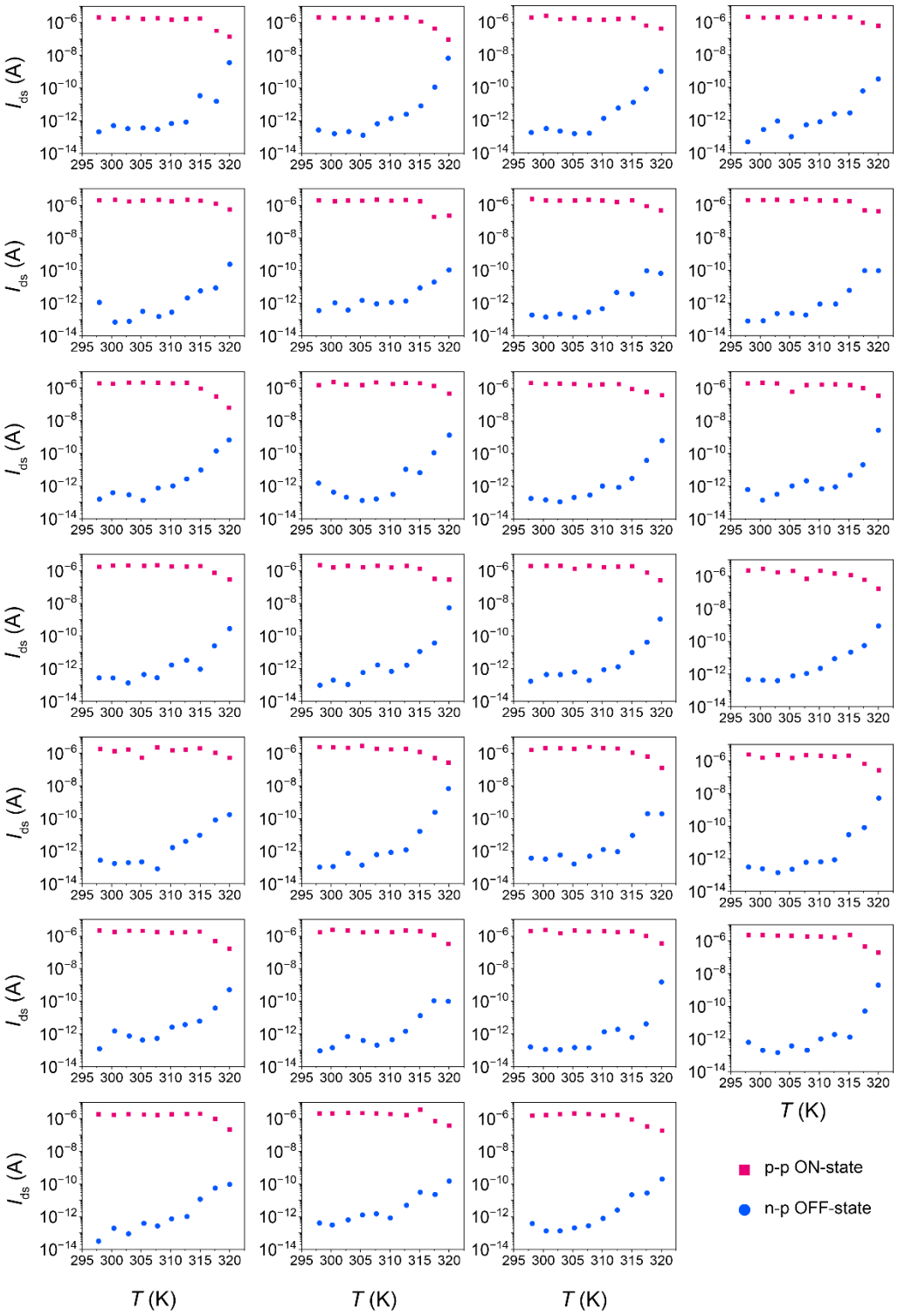


Fig. S43 Temperature-dependent electrical characteristics of the 27-device array. The switching performance of all 27 devices between the ON and OFF states was measured over the temperature range of 298–320 K. The p–p ON current remains near 10^{-6} A with minimal variation below 310 K, and then decreases as the temperature approaches the Curie-region window (315–320 K), consistent with thermally weakened ferroelectric polarization. In contrast, the n–p OFF current shows a mild thermally activated increase.

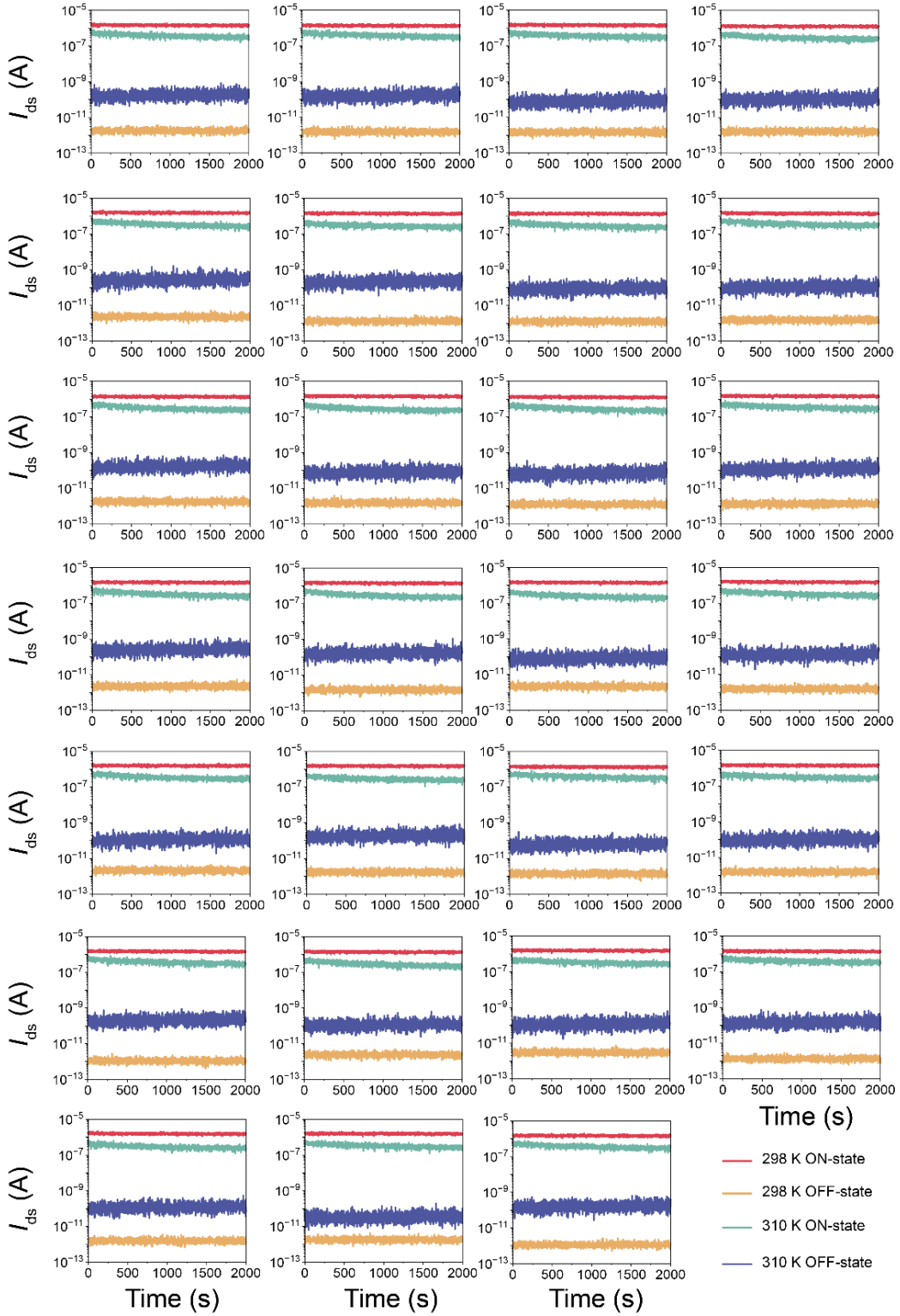


Fig. S44 Retention characteristics of the Fe-FET array under thermal stress. Nonvolatile retention of the programmed ON- and OFF-state currents measured at 298 K and 310 K for all 27 devices. Under elevated-temperature stress (310 K), both conductance states remain stable over the entire measurement window without noticeable drift or state degradation, indicating robust retention and reliable operation at practical operating temperatures.

3.5 Impact of DDV on neural network computation accuracy

To investigate the influence of array-level variability on neuromorphic computing performance, we systematically evaluated the impact of DDV on neural network computation accuracy across various tasks.

Firstly, the functional robustness of the Fe-FET array was validated through a full-hardware implementation of multiband convolution. As shown in fig. S45, broadband images extracted from a hyperspectral dataset were processed using the ISC module, where optical inputs were directly projected onto the array and convolution kernels were realized via spatially programmed photoresponsivity distributions. The resulting photocurrent signals, generated in response to light, directly represent the analog convolution outputs. The experimental results across four visible wavelengths (405 nm, 532 nm, 633 nm, and 755 nm) closely match simulated references, confirming consistent broadband spatial filtering via hardware-native optical computing.

Then, we integrated Fe-FET arrays into a complete CNN comprising ISC, IMC, and NAFs, and evaluated its performance on the MNIST handwritten digit dataset. As shown in Fig. 4D–G, the CNN achieved a recognition accuracy of 95%, closely approaching the software benchmark of 97%. Confusion matrix analysis indicates that most classification errors are minor (fig. S46), demonstrating high robustness despite analog non-idealities.

To quantitatively assess the impact of variability, we also performed systematic simulations by independently varying DDV in analog weights ($DDV_{weights}$, corresponding to ISC and IMC layers) and in NAF response (DDV_{NAFs}) from 0% to 30%. As shown in fig. S47A–C, the CNN maintains high classification accuracy (>90%) when $DDV_{weights}$ remains below 10% and DDV_{NAFs} below 25%, indicating strong tolerance to moderate device variation. Under our experimentally measured DDVs ($DDV_{weights} \approx 5\%$, $DDV_{NAFs} \approx 5\%$), the simulated network achieved a recognition accuracy of 95%, in excellent agreement with the hardware experimental results (Fig. 4G).

To further assess the applicability of our Fe-FET arrays in large-scale neuromorphic

systems and more complex visual tasks, we conducted simulations using deeper CNN models for the CIFAR-10 image classification benchmark. As shown in fig. S47 (D and E), the ideal network configuration achieved a recognition accuracy of approximately 90% after 50 training epochs. When experimentally extracted DDVs were incorporated into the model ($DDV_{weights} \approx 5\%$, $DDV_{NAFs} \approx 5\%$), the classification accuracy remained above 88%, closely matching the ideal case. These results demonstrate that the proposed hardware platform retains strong computational robustness and scalability, even under increased network depth and task complexity.

These results demonstrate that our Fe-FET arrays possess sufficient uniformity to support accurate and robust neuromorphic inference under both simple and complex workloads. The array-level consistency in both analog weights and activation responses ensures computational fidelity, and provides a practical and scalable foundation for future hardware-based embodied vision systems.

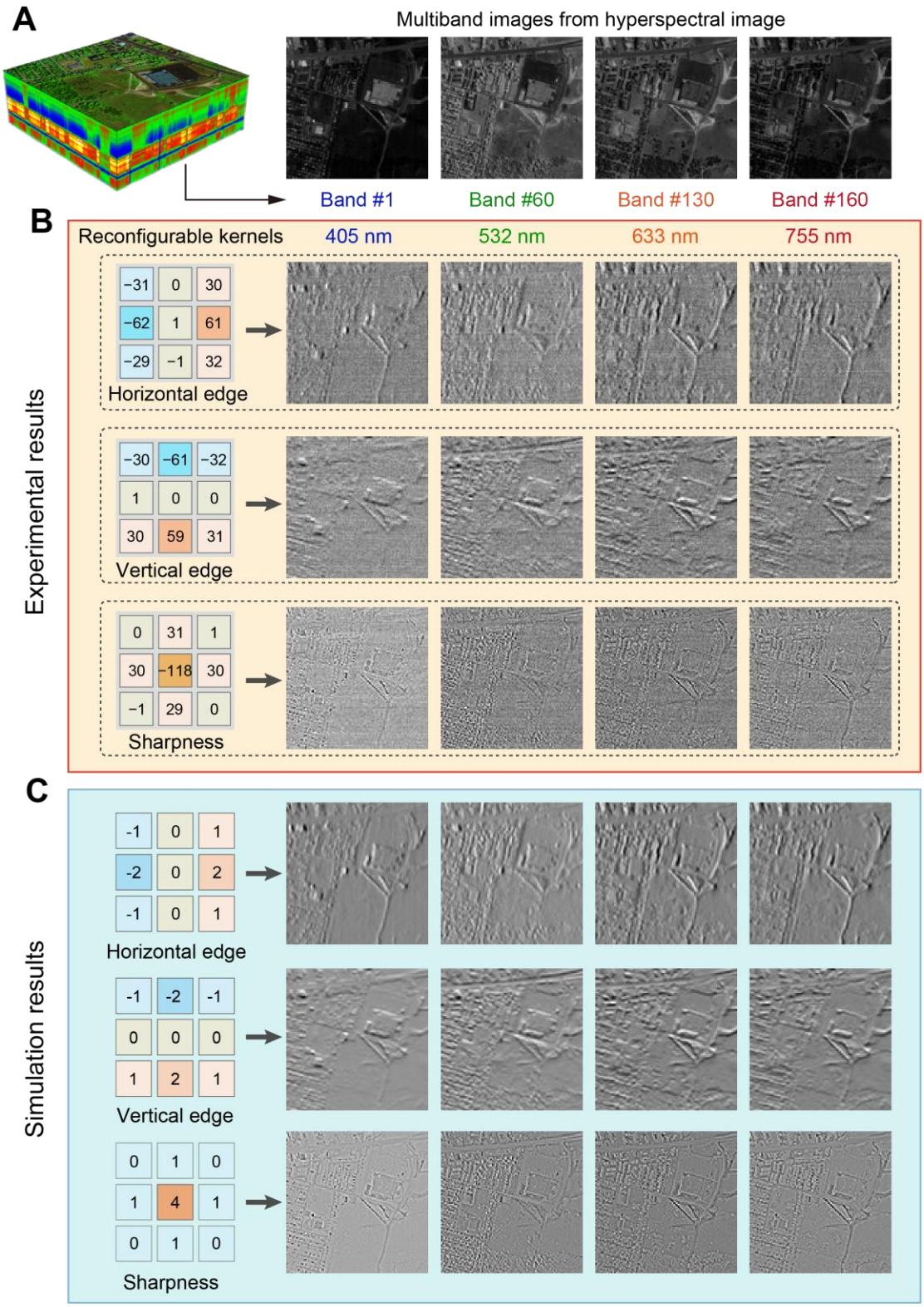


Fig. S45 Broadband convolution processing using the Fe-FET ISC array. (**A**) Representative hyperspectral image slices extracted at 405 nm, 532 nm, 633 nm, and 755 nm from a multiband dataset. Hyperspectral image of Urban is obtained from a public dataset (https://lesun.weebly.com/hyperspectral-data-set.html) (**B**) Experimental convolution results obtained using the ISC array with three spatially programmed

photoresponsivity kernels: horizontal edge, vertical edge, and sharpening. Broadband optical inputs were directly projected onto the array, and the resulting photocurrents reflect kernel-specific analog convolution outputs. (**C**) Software-simulated convolution results using the same kernels, serving as a reference. The close agreement between experimental and simulated outputs validates the accuracy, uniformity, and broadband functionality of the ISC module for direct optical convolution.

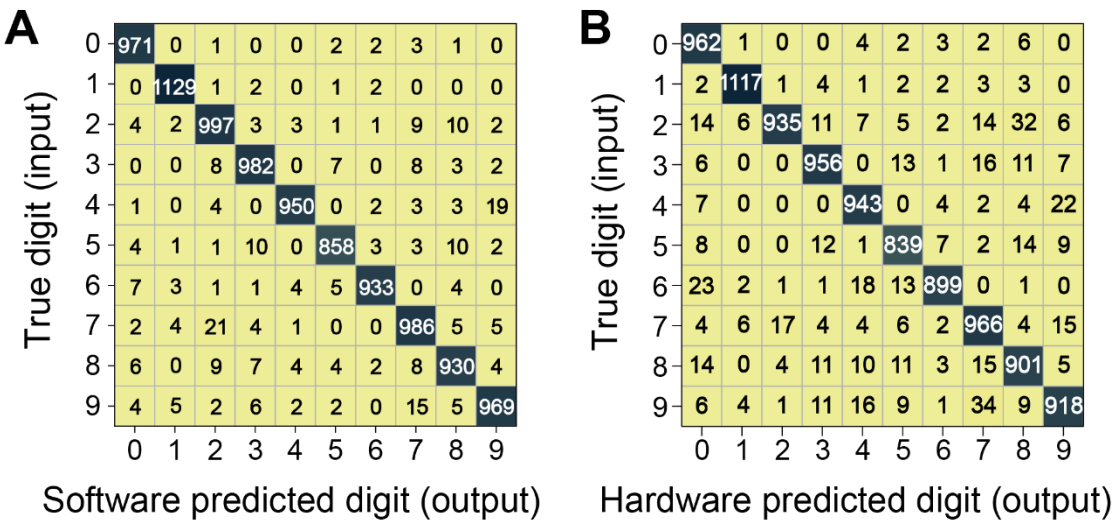


Fig. S46 Confusion matrix of software and hardware CNN classification results on MNIST. (**A**) Confusion matrix of the software-implemented CNN for handwritten digit classification. (**B**) Confusion matrix of the hardware-implemented CNN based on Fe-FET arrays incorporating ISC, IMC, and NAF functionalities. Both systems were evaluated on the MNIST test set. The software CNN achieved a classification accuracy of 97%, while the all-hardware implementation reached 95%, with most errors occurring between visually similar digits. These results demonstrate that the Fe-FET-based neuromorphic hardware can achieve near-software-level performance, validating its accuracy and functional completeness in practical inference tasks.

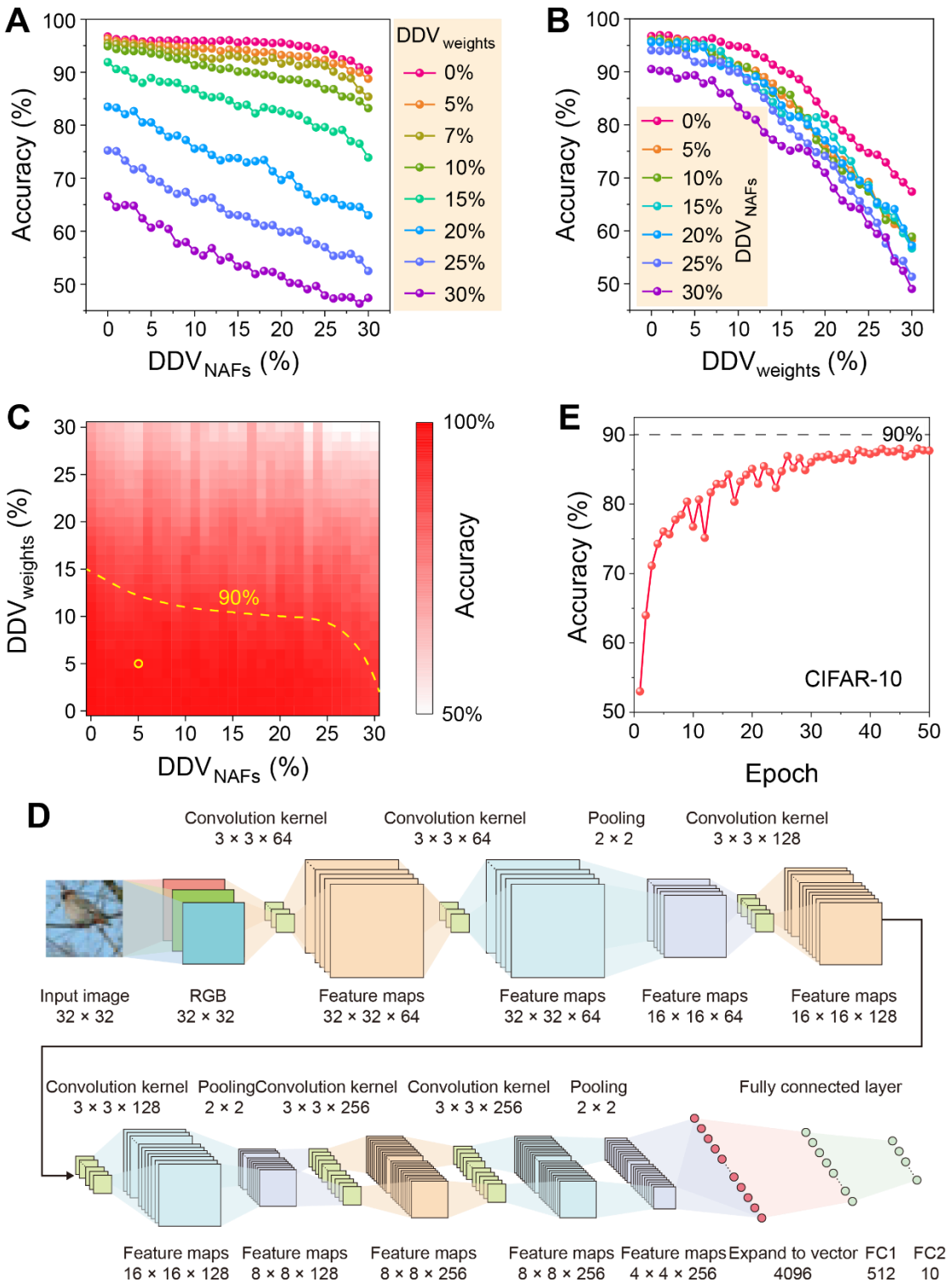


Fig. S47 Simulated impact of device-level variability on CNN inference accuracy. (**A** and **B**) Simulated classification accuracy of a Fe-FET-based CNN on the MNIST dataset under independently varied DDVs in analog weights (DDV_{weighs}, corresponding to ISC and IMC layers) (**A**) and NAFs (DDV_{NAFs}) (**B**). (**C**) Distribution of recognition accuracy for the CNN with different $DDV_{weights}$ and DDV_{NAFs} parameters. The yellow dashed line marks the 90% accuracy threshold, and the yellow circle denotes the

experimentally measured DDV values ($DDV_{weights}$ = 5%, DDV_{NAFs} = 5%). (**D**) Schematic of a deeper CNN model used for CIFAR-10 image classification to assess scalability. (**E**) Accuracy evolution during 50 training epochs, showing a final accuracy of 88% when using experimental DDVs, compared to 90% under ideal device conditions (dashed line). These results confirm that the system maintains high recognition accuracy and robustness even under realistic device variation and increased network complexity.

Supplementary Note 4. System-level implementation and energy analysis of the Fe-FET-based embodied neuromorphic vision system

4.1 System architecture and processing pipeline

To demonstrate the feasibility of monolithically integrating ISC, IMC, and NAFs within a unified hardware platform, we developed a prototype neuromorphic vision system based on reconfigurable Fe-FET arrays. The hardware architecture was implemented on a custom printed circuit board (PCB), incorporating three core functional arrays (ISC, IMC, and NAFs), a field-programmable gate array (FPGA) with onboard DAC/ADC modules, analog multiplexers (MUXs), and a series of TIAs.

Inference pipeline

Fig. S48 (A–C) illustrates the overall system wiring and optical layout, showing the complete analog signal chain of ISC → TIA_{ISC} → ReLU → TIA_{ReLU} → IMC → TIA_{IMC} → Sigmoid → $TIA_{Sigmoid}$. As shown in fig. S48 (D and E), input images are optically projected onto the ISC array using a spatial light modulator (SLM). Each Fe-FET in the ISC array converts localized light intensity into photocurrent, with the photoresponsivity programmed and retained via non-volatile CIPS ferroelectric polarization. The ISC array operates in a self-powered mode without any external bias. As shown in Fig. S49, the 3 × 3 × 3 ISC array is divided into three groups, where devices sharing identical subpixel indices (m = 1, 2, 3) are connected in parallel to generate three nA-level photocurrents (I_1, I_2, I_3). These analog currents are converted into voltage signals (V_1, V_2, V_3, –1 V to +1 V) by the TIA_{ISC}, which subsequently serve as $V_{in,ReLU}$ inputs to the hardware NAF array for ReLU activation. The activated outputs are transmitted via another amplifier stage (TIA_{ReLU}) to the IMC array, maintaining a 0–1 V dynamic range. The 3 × 9 IMC array, whose configuration is shown in Fig. S50, produces nine sub-μA output currents corresponding to analog MVM operations. These output currents are converted into 0–1 V voltage signals by TIA_{IMC} and then fed into the Sigmoid-type NAF array for the final nonlinear activation. The resulting output voltages (0–1 V) from the $TIA_{Sigmoid}$ are collected by the FPGA and used for real-time

classification and image reconstruction tasks. All functional arrays can be individually programmed or reconfigured by write pulses controlled by the FPGA and routed through MUXs.

End-to-end inference latency

In our setup, the ISC device exhibits a rise time of ~440 ns for optical excitation, which dominates the pipeline latency. The IMC and NAF devices (both ReLU and Sigmoid modes) respond with ~8 ns each under optimized bias. The signal path contains four TIA stages (TIA_{ISC}, TIA_{ReLU}, TIA_{IMC}, and $TIA_{Sigmoid}$). At the operational gains used here, each TIA contributes a 5–20 ns settling time (nanosecond-scale rise, propagation delay <5 ns). Accordingly, the end-to-end latency per inference sample is < 0.6 μs.

Training and weight update procedure

During training, the system executes supervised or unsupervised learning tasks by iteratively updating the weights of Fe-FETs operating in either ISC or IMC mode. As illustrated in fig. S48A, optical inputs are delivered to the ISC array, and the resulting signals sequentially propagate through the ReLU-NAF, IMC, and Sigmoid-NAF arrays to generate predicted outputs. These outputs are digitized and compared with target labels by the FPGA to compute the loss function. Error gradients are backpropagated to determine the required weight updates.

Each Fe-FET features two independently addressable control gates, allowing separate programming of photoresponsivity (for ISC) and conductance (for IMC). Weight updates are executed in a closed-loop manner by delivering ±3 V, 100 ns electrical pulses to the control gates, routed through the MUX network. This enables targeted and efficient in situ programming of individual devices.

In our current hardware setup, the FPGA board integrates a dual-channel DAC, enabling the simultaneous programming of both control gates within a single device. Thus, updating one Fe-FET device require a single 100 ns operation. For a 27-device array (comprising 54 control gates), sequential reprogramming completes within

approximately 2.7 μs. Considering peripheral overhead—including DAC settling time, MUX switching delay, and FPGA address decoding—the total training update latency is estimated at 10–20 μs per full array update.

Signal conditioning and noise performance

To ensure consistent signal scaling across current domains spanning from nA (ISC/Sigmoid) to μA (IMC/ReLU), each TIA is configured with a transimpedance gain matched to its corresponding module:

For the ISC array, the output photocurrent corresponds to the cumulative response of nine parallel-connected Fe-FET devices (fig. S49), typically around 100 nA. Accordingly, a TIA_{ISC} with a gain of 10^7 V A^{-1} is used.

For the IMC array, the output current arises from three parallel-connected devices (fig. S50), typically around 10 μA, and is processed using a TIA_{IMC} with a gain of 10^5 V A^{-1}.

For the ReLU and Sigmoid activation arrays, the output currents are approximately 2 μA and 10 nA, respectively, corresponding to TIA gains of 5×10^5 V A^{-1} and 10^8 V A^{-1}.

The input-referred noise floor of the TIAs is below 0.8–65 fA $Hz^{-1/2}$, ensuring that the amplification process introduces negligible noise and preserves a nearly lossless signal-to-noise ratio across all current domains.

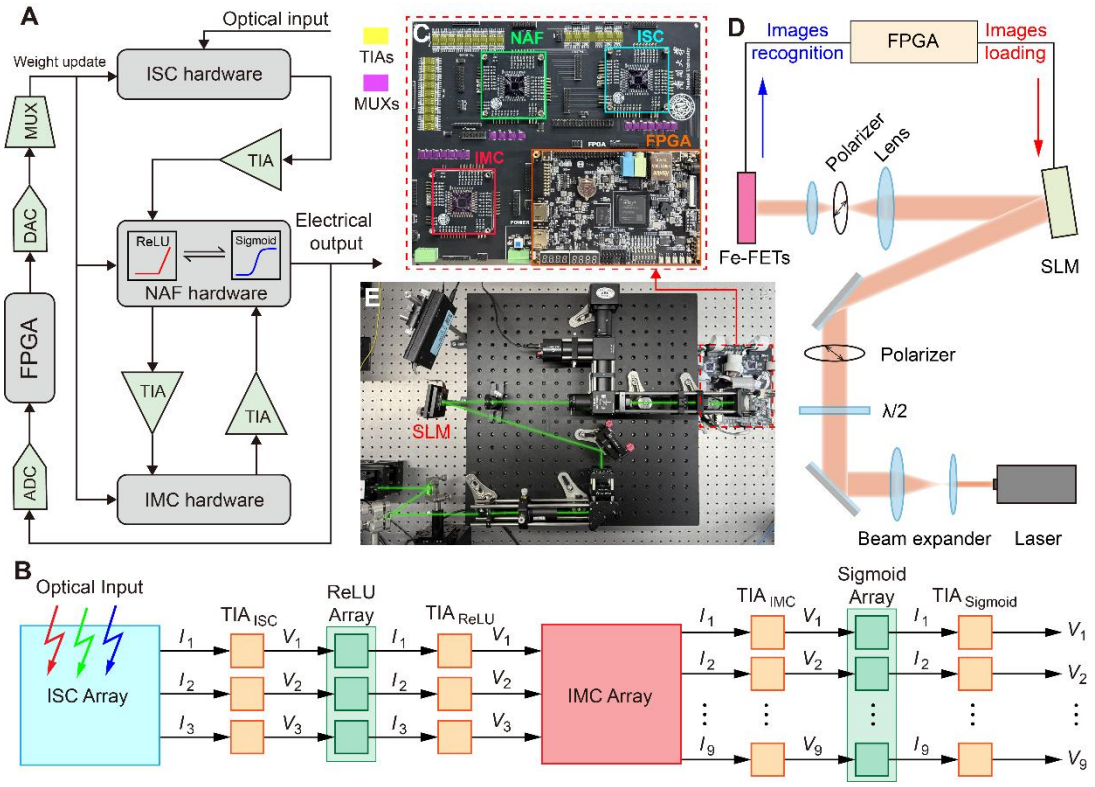


Fig. S48 System architecture and experimental setup for Fe-FET–based embodied neuromorphic vision. (**A**) Schematic of the integrated hardware system comprising ISC, NAF, and IMC modules, along with FPGA, MUXs, and TIAs. The system supports both training and inference via electrical or optical input/output pathways. (**B**) Signal flow diagram of the end-to-end analog computing pipeline. Optical images are projected onto the ISC array to generate photocurrents (I_1–I_3), which are converted into voltage signals (V_1–V_3) by TIA_{ISC} and transmitted to the ReLU-type NAF array. The activated signals are further processed through TIA_{ReLU}, input into the IMC array for MVM. The nine output currents (I_1–I_9) are finally passed through TIA_{IMC}, the Sigmoid-type NAF array and $TIA_{Sigmoid}$ to produce output voltages (V_1–V_9) for classification or image reconstruction. The overall signal chain follows: ISC → TIA_{ISC} → ReLU → TIA_{ReLU} → IMC → TIA_{IMC} → Sigmoid → $TIA_{Sigmoid}$. (**C**) Photograph of the hardware prototype implemented on a multi-module PCB. The ISC, IMC, and NAF Fe-FET arrays are highlighted, with integrated FPGA controller and peripheral circuitry. (**D**) Schematic of the optical system used for image loading and recognition. A laser source is expanded and modulated by a SLM before being projected onto the Fe-FET array. Polarizers and lenses are used to control the beam profile and polarization. (**E**) Photograph of the optical setup corresponding to the schematic in (**D**), showing beam path routing and key optical elements.

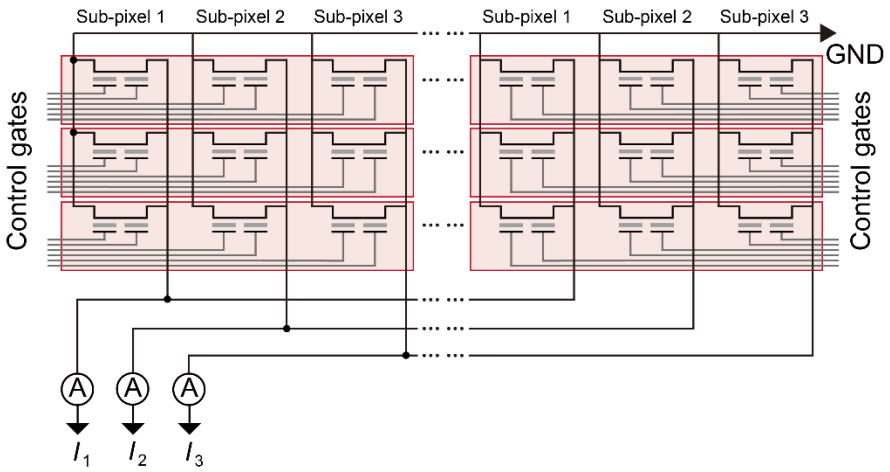


Fig. S49 Circuit schematic of the 3 × 3 × 3 Fe-FET ISC array. The ISC array consists of 3 × 3 pixels, each composed of three Fe-FET sub-pixels (Sub-pixel 1–3). Devices with identical sub-pixel indices (m = 1–3) across the array are connected in parallel to produce three summed photocurrent outputs (I_1, I_2, and I_3). These currents are subsequently converted into voltage signals through the transimpedance amplifier stage (TIA_{ISC}) for input to the ReLU-type NAF array. The ISC operates in a self-powered mode without any external bias, where incident light alone drives the photocurrent generation. Each Fe-FET's photoresponsivity is non-volatilely programmed via the ferroelectric polarization state of its underlying CIPS layer and remains stable during inference. The dual control gates (CG_1, CG_2) on each device allow independent addressing and localized programming through the MUX-controlled circuitry, enabling precise adjustment of photoresponsivity or spatial weighting across the array. This configuration allows the ISC array to perform spatially parallel analog convolution directly in the sensory terminal, generating three channel-specific photocurrent outputs that serve as hardware-native feature maps for subsequent neuromorphic processing.

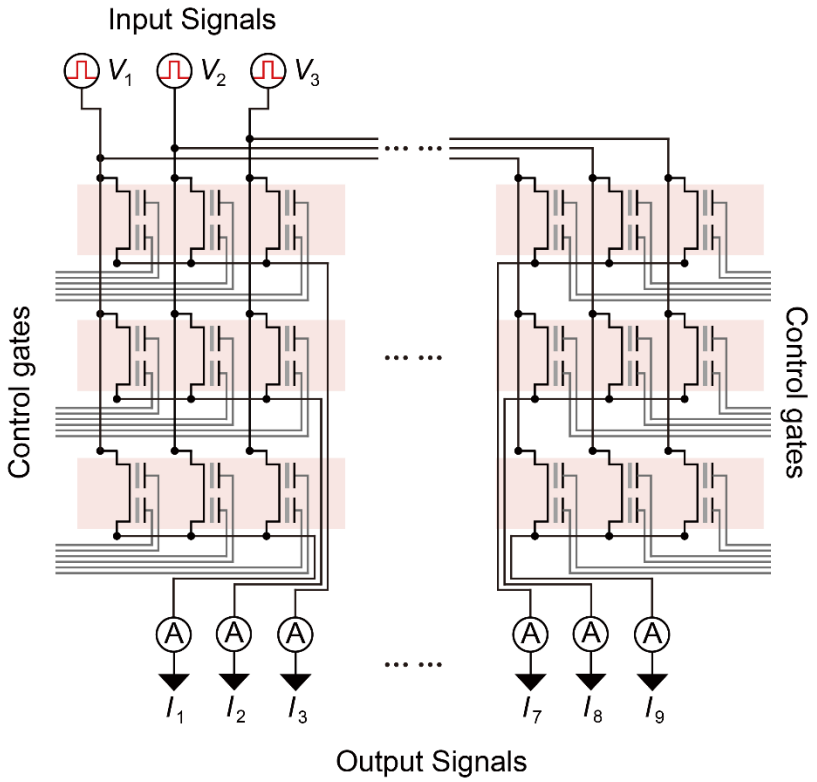


Fig. S50 Circuit schematic of the 3 × 9 Fe-FET IMC array. The IMC array consists of three input lines (V_1–V_3) and nine output columns (I_1–I_9), forming a reconfigurable 3 × 9 crossbar structure for analog MVM. Each Fe-FET device serves as a programmable analog synapse, where the channel conductance—representing the synaptic weight—is precisely tuned through ferroelectric polarization control of the underlying CIPS layer. During inference, the input voltages (V_1–V_3) corresponding to ReLU-activated outputs are applied to the word lines, while the resulting analog output currents (I_1–I_9) are collected along the shared bit lines. These output currents naturally implement the weighted-sum operation at the device level and are subsequently converted into voltage signals by the TIA_{IMC} stage for further nonlinear activation through the Sigmoid NAF array. Each Fe-FET incorporates dual, independently addressable control gates that allow selective in situ programming and reconfiguration of individual synaptic weights via ±3 V, 100 ns voltage pulses routed through the MUX network. This architecture enables continuous, low-energy, and non-volatile weight tuning while preserving high linearity and uniformity across the array, providing the essential hardware foundation for scalable analog matrix computation.

4.2 Device-level energy consumption

To assess the energy efficiency of Fe-FETs for neuromorphic hardware deployment, we systematically analyzed their energy consumption across different functional modes, including ISC, IMC, and NAF (ReLU and Sigmoid).

Programming-stage energy consumption

The energy consumption for programming is estimated from the *P–V* loop. In this measurement, CIPS is configured as a metal–ferroelectric–metal (MFM) capacitor and the *P–V* loop is recorded under the same polarization-switching conditions used for device programming (fig. S51). The switching energy is determined from the work done to reverse the ferroelectric polarization charge, which can be expressed as

$$\Delta E = \int_{Q_1}^{Q_2} V dQ = \int_{P_1}^{P_2} V dP \cdot A ,$$

where Q is the polarization charge, $P = Q/A$ is the polarization, and A is the effective switched area of the CIPS layer. Practically, $\Delta E/A$ corresponds to the loop integral $\int V dP$, i.e., the enclosed *P–V* hysteresis area associated with polarization reversal. Using the effective CIPS area in our Fe-FET (A = 10 μm^2), we obtain intrinsic switching energies of ~1.49 pJ and ~1.40 pJ for the positive and negative programming processes, respectively.

This estimation captures the intrinsic energy associated with ferroelectric polarization switching, which constitutes the dominant and fundamental energy cost of the programming process in ferroelectric-based devices. It therefore provides a physically meaningful and widely adopted metric for evaluating the energy efficiency of ferroelectric switching. Nevertheless, it should be noted that, in an actual Fe-FET device, the total programming energy may additionally include contributions from gate charging, parasitic capacitances, leakage currents, and channel-related effects, which are not captured in the present MFM-based measurement.

Inference-stage energy consumption

During inference, the Fe-FET performs analog-domain signal processing with extremely low energy consumption. The estimated upper bounds for dynamic energy consumption per operation are:

ISC: zero energy consumption (photovoltaic).

IMC: max ~64 fJ (at 1 V, ~8 μA, 8 ns).

ReLU NAF: max ~16 fJ (at 1 V, ~2 μA, 8 ns).

Sigmoid NAF: max ~ 80 aJ (at 1 V, ~10 nA, 8 ns).

These results highlight the extreme energy efficiency of the Fe-FET-based platform, making it highly suitable for edge AI applications with stringent power budgets. The above values represent the intrinsic device-level energy, excluding peripheral overheads.

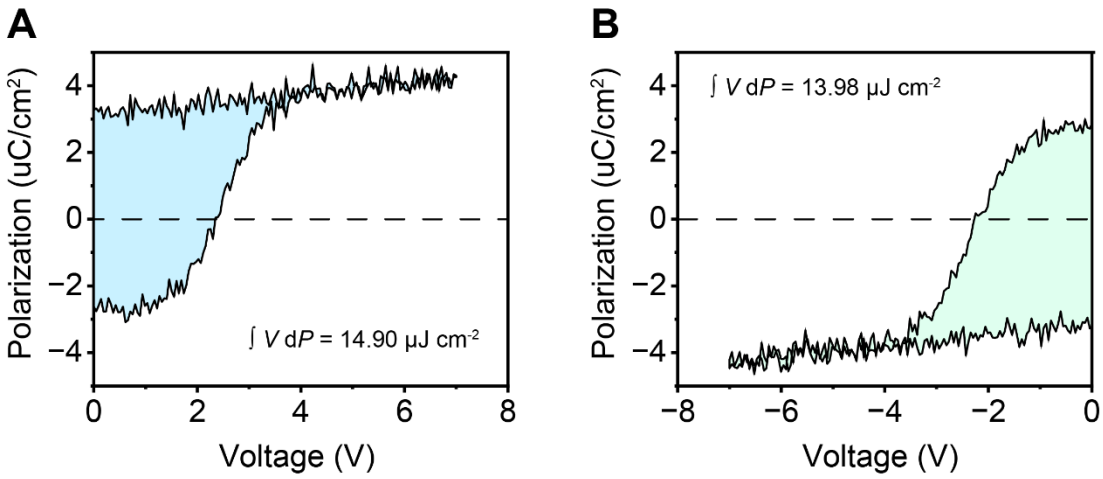


Fig. S51 Quantification of intrinsic ferroelectric switching energy in CIPS. Polarization–voltage (*P*–*V*) hysteresis loops measured from a metal–ferroelectric–metal CIPS capacitor under positive (**A**) and negative (**B**) programming polarity. The shaded areas represent the switching work density, $\int VdP$, extracted from the loop integral during polarization reversal (values indicated in each panel). Using an effective switched area of 10 μm^2, the corresponding intrinsic switching energies are calculated to be ∼1.49 pJ and ∼1.40 pJ for the positive and negative programming processes, respectively.

4.3 System-level energy analysis

To evaluate the practical energy performance of the Fe-FET-based embodied neuromorphic vision system, we performed a comprehensive analysis of system-level energy consumption during both inference and training/configuration.

Inference-stage energy consumption

During inference, the system operates as follows:

- Optical input is projected onto the ISC array, which passively generates photocurrent.
- The outputs are processed through 3 TIAs and fed into the ReLU-NAF array.
- The ReLU outputs are again processed through 3 TIAs before reaching the IMC array.
- IMC computation generates 9 outputs, each fed into a TIA and subsequently into the Sigmoid-NAF array.

A total of **15 TIAs** are used during inference, accounting for the dominant energy overhead. The energy breakdown is summarized below:

Component	Number of units	Energy per unit	Total energy
ISC computation	27 devices	0 (photovoltaic)	0
TIA (ISC→ReLU)	3	8 pJ	24 pJ
ReLU activation	3 devices	16 fJ	48 fJ
TIA (ReLU→IMC)	3	8 pJ	24 pJ
IMC computation	27 devices	64 fJ	1.7 pJ
TIA (IMC→Sigmoid)	9	8 pJ	72 pJ
Sigmoidal activation	9 devices	80 aJ	0.7 fJ
Total			**121.7 pJ**

Thus, each inference cycle consumes only ~121.7 pJ, even when accounting for peripheral circuit overhead.

Training-stage energy consumption

Training involves updating the photoresponsivity of 27 ISC devices, the conductance of 27 IMC devices, and the NAF characteristics of 12 devices (3 ReLU + 9 Sigmoid). The total device-level training energy is:

- ISC: 27 × 2.89 pJ = 78.0 pJ
- IMC: 27 × 1.49 pJ = 40.2 pJ
- NAF: 12 × 2.89 pJ = 34.7 pJ
- **Total**: **152.9 pJ**

This analysis confirms that both the inference and training operations are performed at exceptionally low energy costs, supporting scalable and energy-efficient deployment of the Fe-FET-based neuromorphic system.

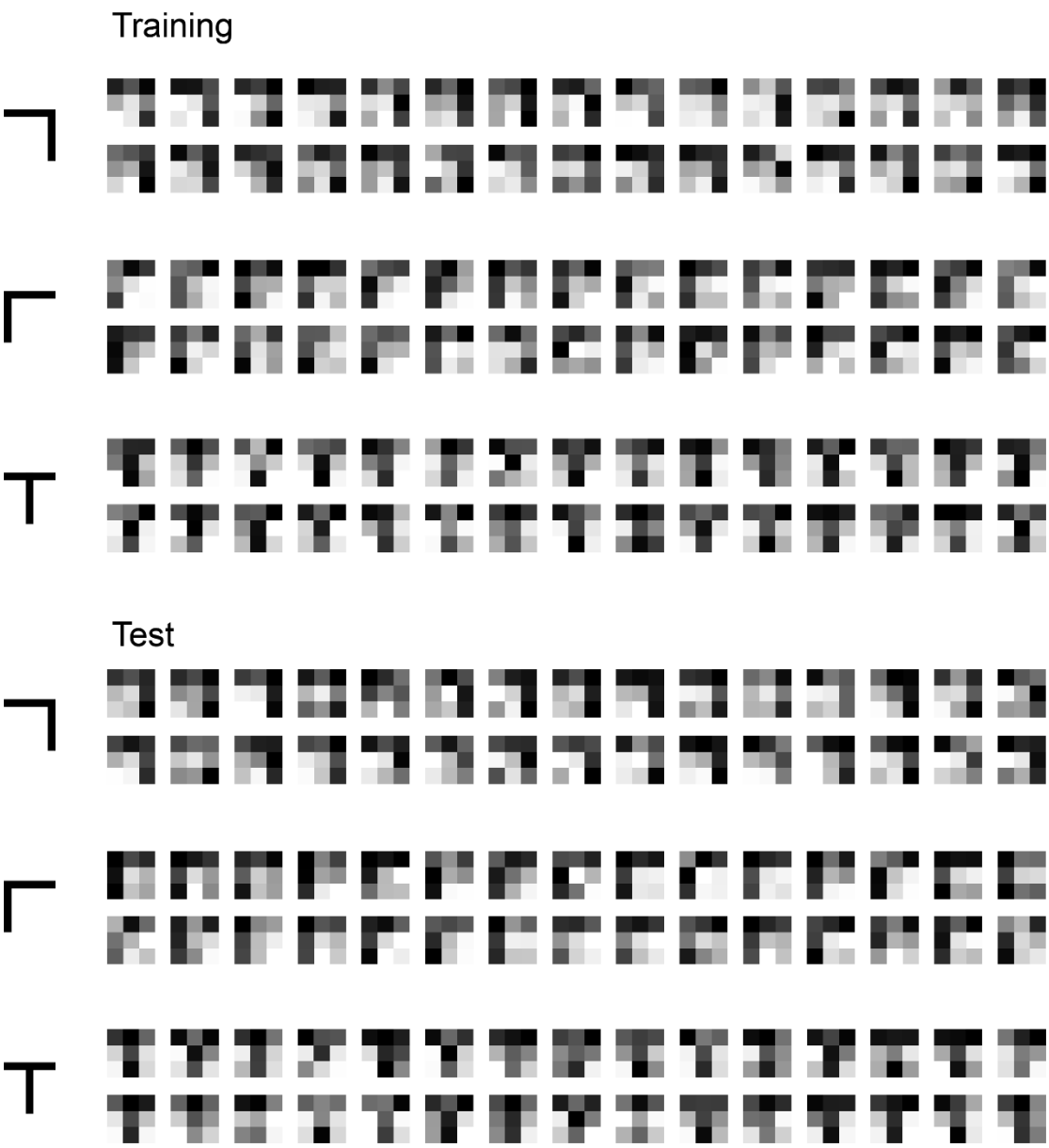


Fig. S52 Custom symbolic dataset used for classification and autoencoding tasks. Example images from the training and test sets of a custom 3 × 3-pixel symbolic dataset. The dataset includes three classes (‘ㄱ’, ‘ㄷ’, and ‘ㅜ’), each corrupted with randomly generated noise to simulate real-world distortions. A total of 600 images were used for training and 150 for testing. This dataset was employed to evaluate the performance of the Fe-FET-based system on both supervised classification and unsupervised reconstruction tasks.

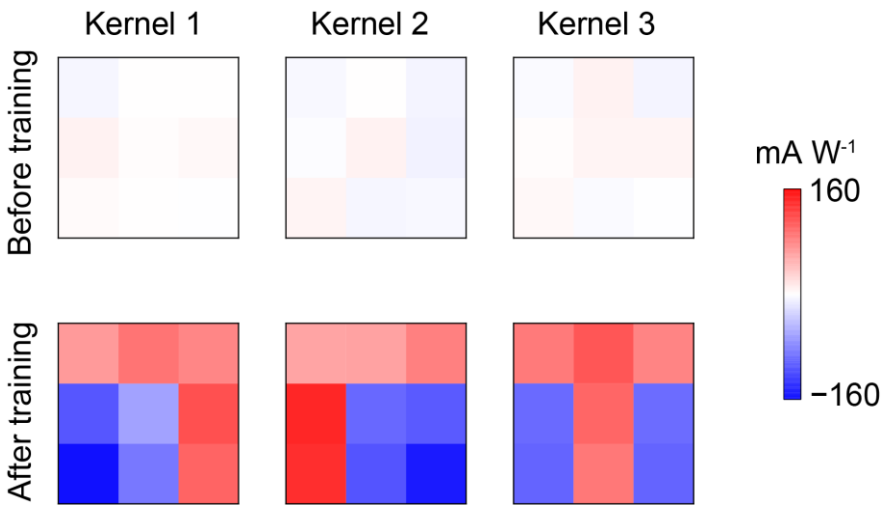


Fig. S53 Photoresponsivity distributions of the ISC array before and after training for classification tasks. Spatial distributions of photoresponsivity in three 3 × 3 convolution kernels used in the classifier module. The top row shows the initial (randomized) states prior to training, while the bottom row displays the learned photoresponsivity maps after training. Distinct positive and negative values emerge in the trained kernels, enabling effective feature extraction from symbolic image inputs.

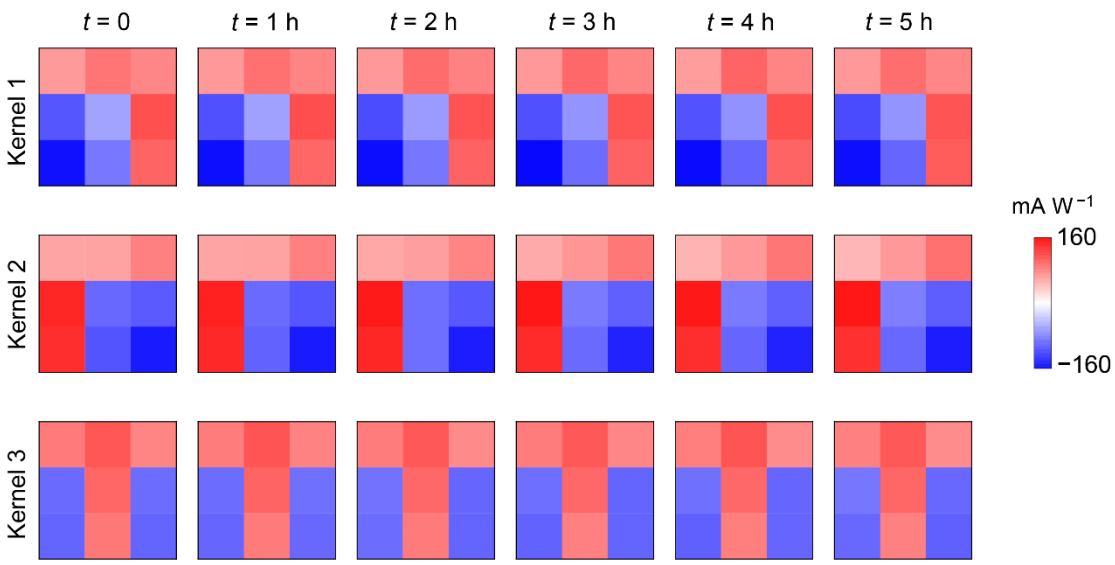


Fig. S54 Retention characteristics of trained photoresponsivity in the ISC array. Temporal evolution of the photoresponsivity maps for three trained convolution kernels over a 5-hour duration. Each kernel comprises a 3 × 3 subarray of Fe-FETs configured in ISC mode. The spatial distributions remain highly stable over time, indicating excellent nonvolatile retention of optical weights after training.

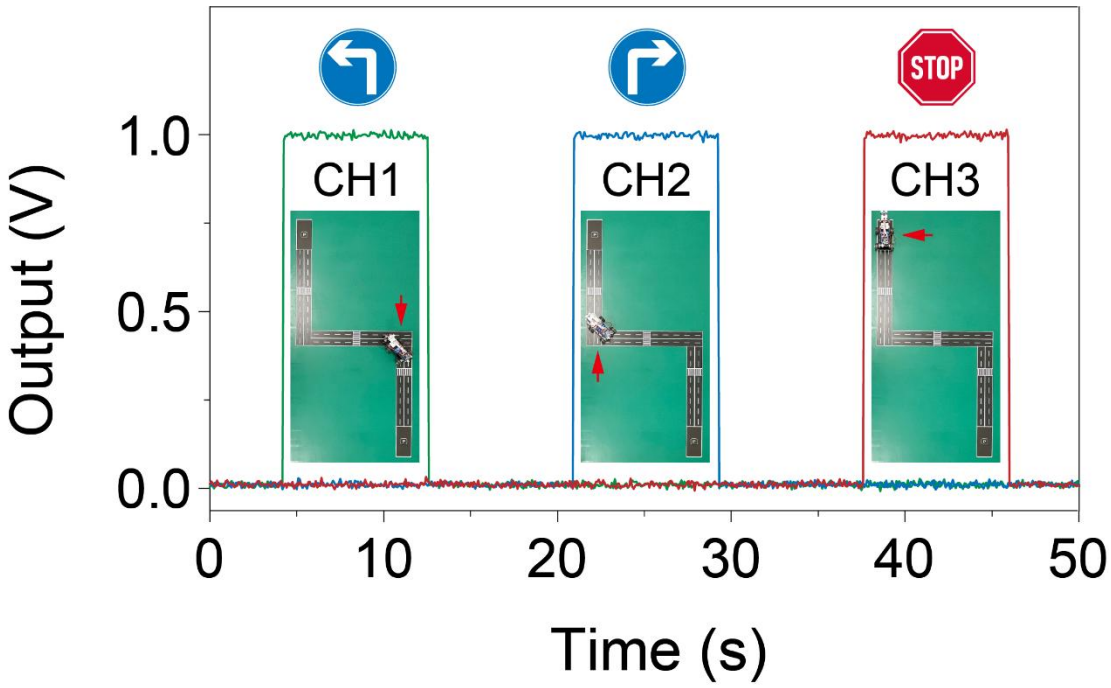


Fig. S55 Real-time robot control enabled by the trained Fe-FET neuromorphic vision hardware. Time-resolved output voltages from three NAF channels (CH1–CH3) during on-board traffic-sign recognition. When a given sign is detected, the corresponding channel output rises to ~1 V while the other channels remain near baseline, triggering the associated action (left turn for CH1, right turn for CH2, and stop for CH3). Insets show representative robot-car snapshots at the activation moments (red arrowheads).

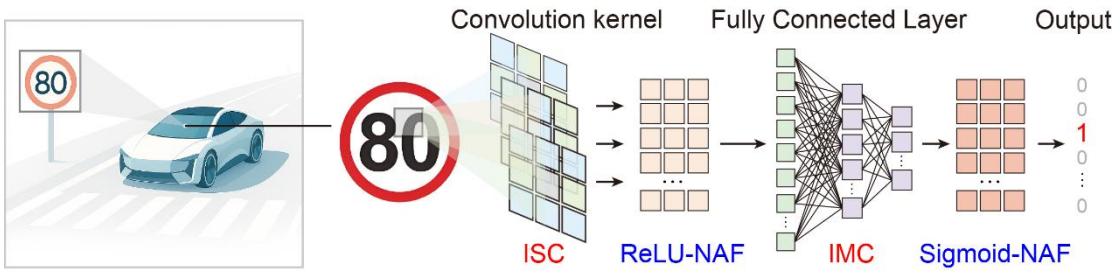


Fig. S56 Schematic of the traffic-sign recognition pipeline implemented on the reconfigurable Fe-FET hardware. The input traffic-sign image is first processed by an ISC array configured for convolutional feature extraction, followed by ReLU-type Fe-FET activations. The resulting feature vector is then fed into an IMC array for fully connected matrix–vector computation, and a Sigmoid-type Fe-FET NAF produces the final probability outputs for classification.

Fig. S57 Representative samples from the Traffic-Signs Dataset. Examples of the 14 traffic-sign categories used in this work, selected from the Kaggle Traffic-Signs-Dataset (https://www.kaggle.com/code/rabbitcuteking/traffic-signs-recognition/input). All images were uniformly preprocessed into 32 × 32-pixel grayscale or RGB inputs before being fed into the Fe-FET hardware system. The full dataset contains 2475 images in total, with 2317 images used for training and 158 images reserved for testing. Categories include speed-limit signs, directional indicators, prohibitory signs, and cautionary symbols, as illustrated in rows 1–14.

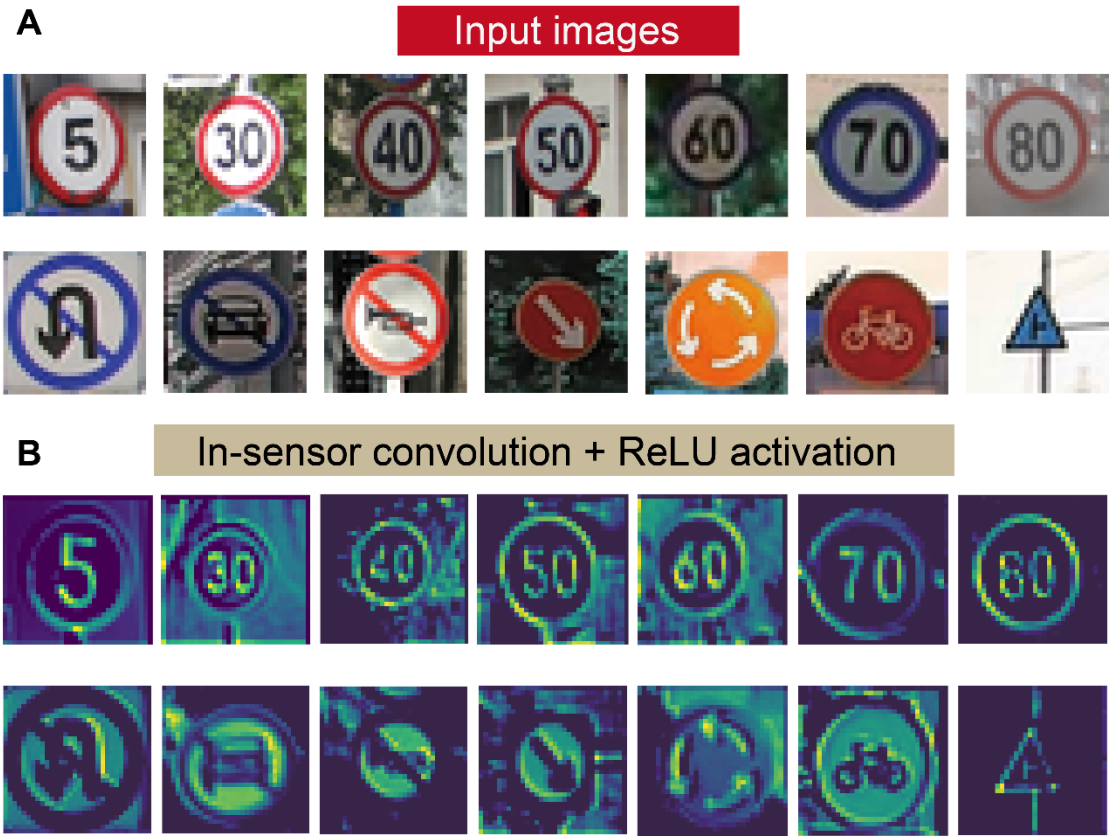


Fig. S58 Raw traffic-sign inputs and hardware-processed feature maps using in-sensor convolution and ReLU activation. (**A**) Representative 32 × 32-pixel input images from the 14-category Traffic-Signs-Dataset used for real-world visual recognition. Each image is first projected to the Fe-FET ISC module, where spatial convolution is performed directly within the phototransistor array by programming position-dependent photoresponsivity kernels. The convolved outputs are then routed through ReLU-type Fe-FET nonlinear activation to extract high-contrast edge and contour features. (**B**) Resulting hardware-generated feature maps for all 14 categories, demonstrating effective in-sensor convolution and nonlinear activation, and forming the first stage of the end-to-end Fe-FET neuromorphic vision pipeline.

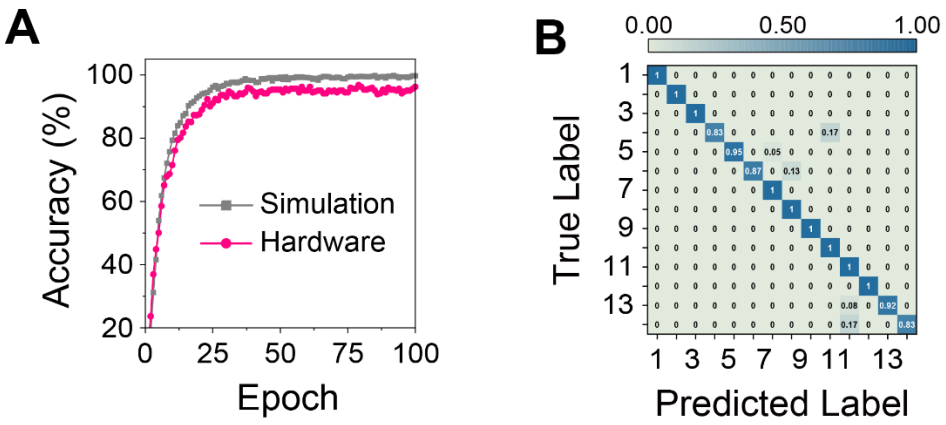


Fig. S59 Traffic-sign recognition on the Kaggle Traffic-Signs-Dataset (32 × 32 pixels, 14 categories). (A) Classification accuracy versus training epoch for software simulation (gray) and Fe-FET hardware inference (magenta), showing comparable convergence behavior and final accuracy. **(B)** Confusion matrix of the hardware-recognized results across the 14 traffic-sign categories, indicating robust multi-class classification with high diagonal dominance and limited inter-class confusion.

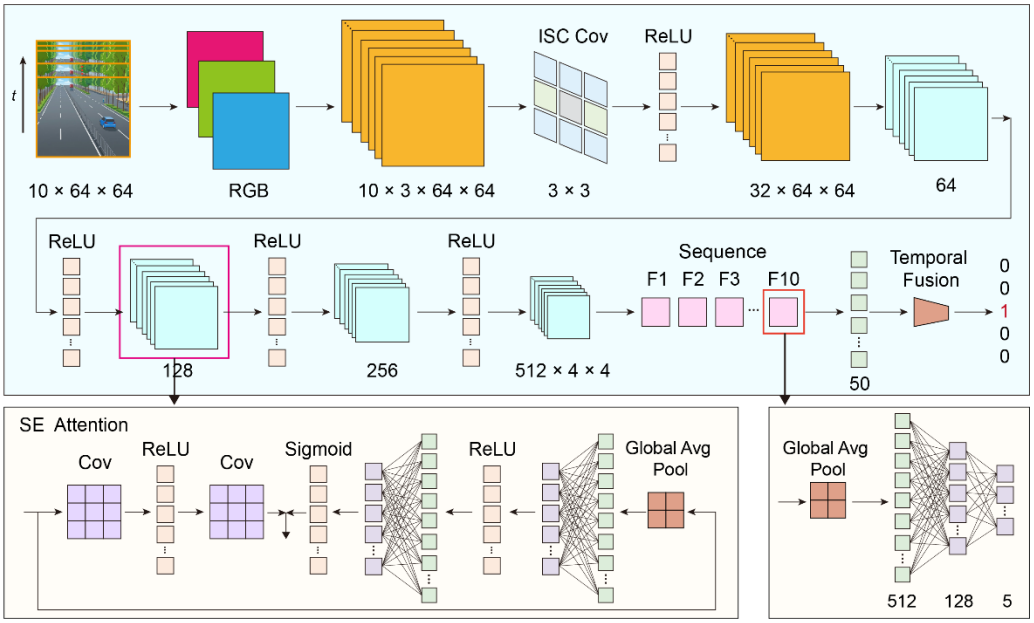


Fig. S60 Neural network mode for UA-DETRAC video processing. A sequence of 10 RGB frames (64 × 64) is first processed by an ISC convolutional front-end using 32 programmable 3 × 3 kernels to generate low-level feature maps, followed by ReLU activation. Deeper feature extraction is then carried out by cascaded IMC stages that implement the main backbone with interleaved ReLU, progressively increasing channel dimension (64 → 128 → 256 → 512) and reducing spatial resolution down to 4 × 4. Within the backbone, SE attention is realized by global average pooling and a Sigmoid gating path to recalibrate channel weights. Frame-wise feature vectors (F1–F10) are subsequently aggregated by a temporal-fusion module to produce the final class decision (probability output).

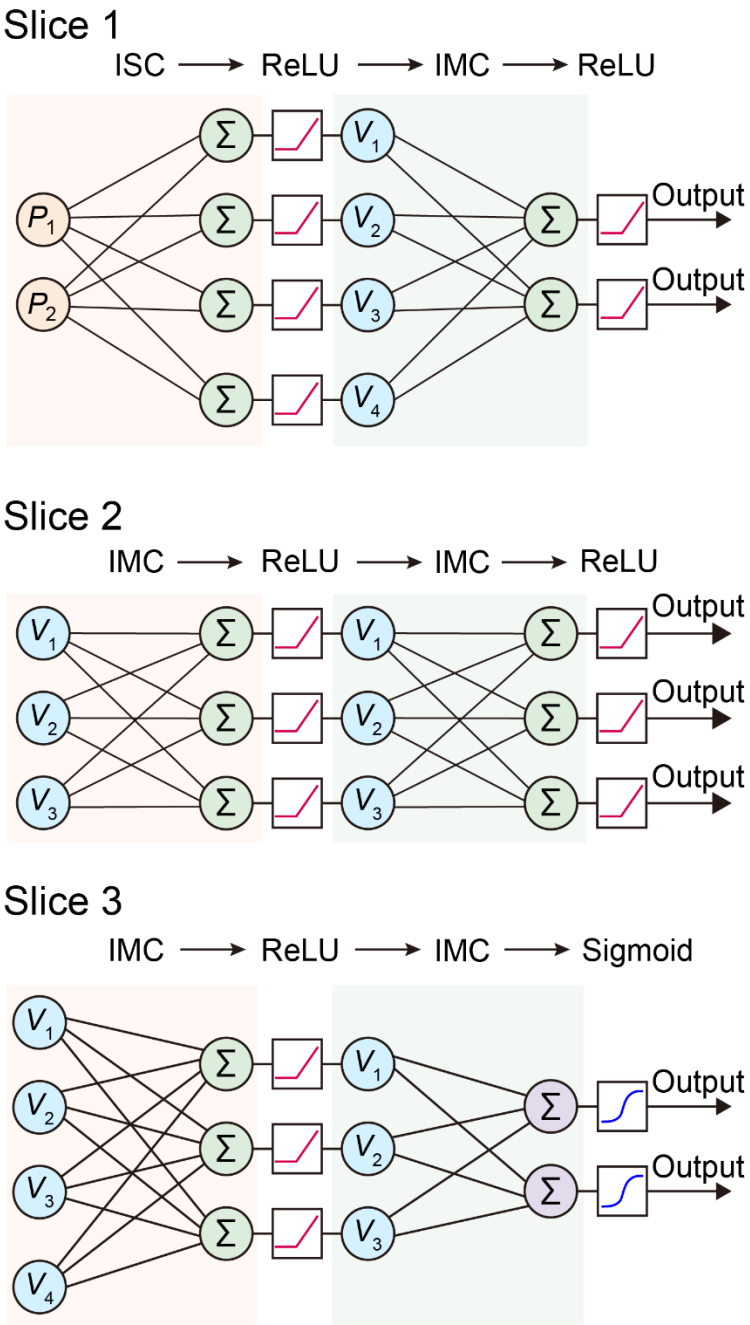


Fig. S61 Task-slicing strategy and corresponding hardware-mapped sub-network configurations. Three representative task slices are extracted from the full model (fig. S60) to fit the available array size while preserving the analog compute chain. Slice 1 spans ISC-based sensory encoding (photocurrent inputs P_1, P_2), followed by ReLU activation and an IMC stage that performs weighted accumulation to generate multi-channel outputs. Slice 2 consists of cascaded IMC stages with an interleaved ReLU, representing a deeper linear–nonlinear computation segment within the network backbone. Slice 3 implements an IMC–ReLU–IMC pipeline with a Sigmoid output activation, emulating the decision/readout stage.

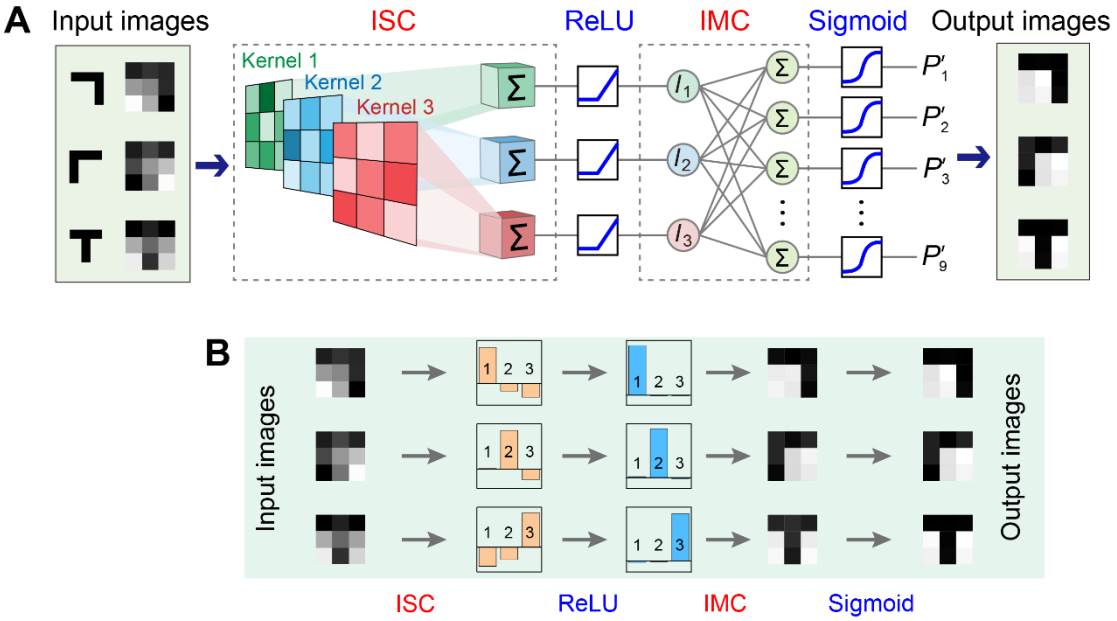


Fig. S62 Hardware implementation of an Fe-FET–based unsupervised autoencoder. (**A**) Schematic illustration of the full-hardware autoencoder constructed using the reconfigurable Fe-FET platform. Input images are first processed by the ISC module, where three programmed 3 × 3 kernels perform analog convolution directly in the phototransistor array. The resulting feature currents pass through ReLU-type Fe-FET nonlinear activation and are then fed into the IMC crossbar to execute the analog fully connected operation. At the output stage, Fe-FETs reconfigured into Sigmoid-type activation generate nonlinear mapping to reconstruct 3 × 3-pixel images, completing the unsupervised encoding–decoding cycle purely in the analog domain. (**B**) Representative input images and their hardware-reconstructed counterparts. The sequential processing pipeline (ISC → ReLU → IMC → Sigmoid) is performed entirely by reconfigurable Fe-FET arrays. The system achieves accurate structural reconstruction of the symbolic patterns, demonstrating the feasibility and robustness of fully hardware-native unsupervised learning using monolithic Fe-FET neuromorphic primitives.

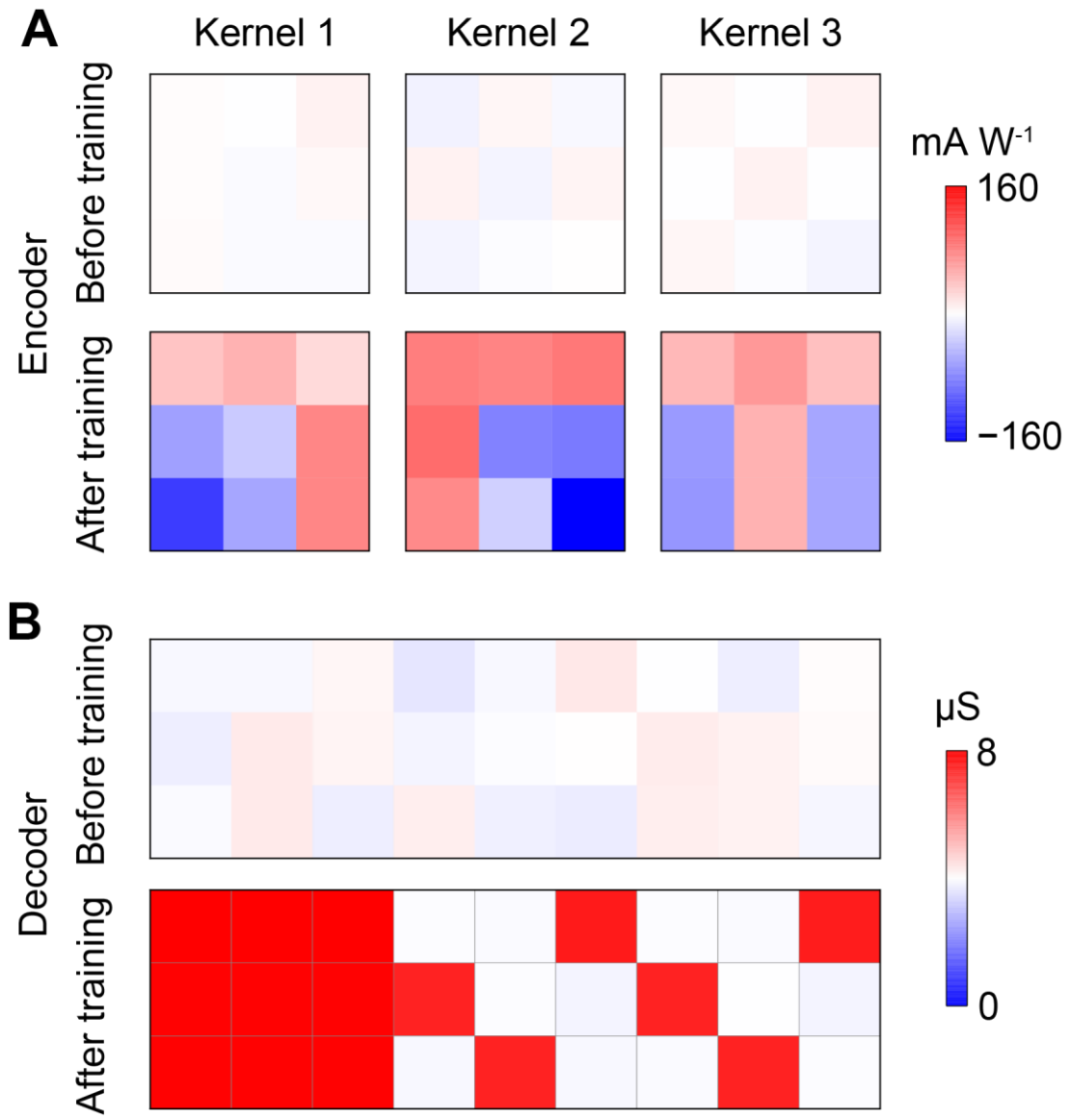


Fig. S63 Weight distributions in ISC and IMC arrays for the autoencoder task. (**A**) Spatial photoresponsivity maps of three ISC kernels (encoder) before and after training, showing clear formation of structured optical weights in the ±160 mA W^{-1} range. (**B**) Corresponding conductance distributions of the IMC decoder array before and after training.

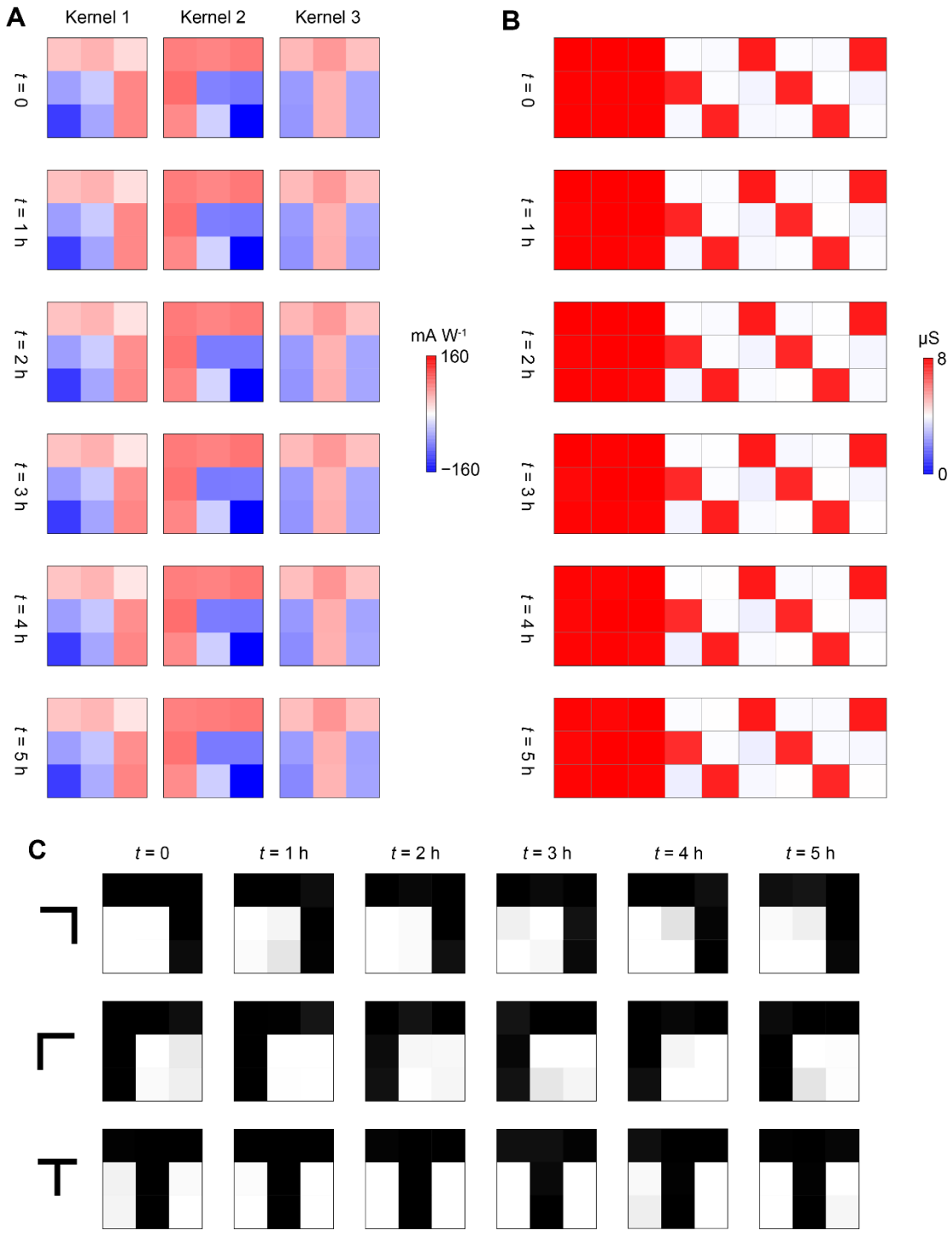


Fig. S64 Retention characteristics of ISC/IMC weights and reconstructed images in the autoencoder task. (**A**) Time-dependent evolution of photoresponsivity distributions in the three trained ISC kernels over 5 hours. (**B**) Corresponding conductance retention maps of the trained IMC array. (**C**) Autoencoder reconstruction results at different retention times. The reconstructed patterns ('ㄱ', 'ㄴ', and 'ㅜ') remain visually stable with structural similarity index (SSIM) exceeding 0.99, demonstrating excellent weight and functional retention of the Fe-FET-based system.

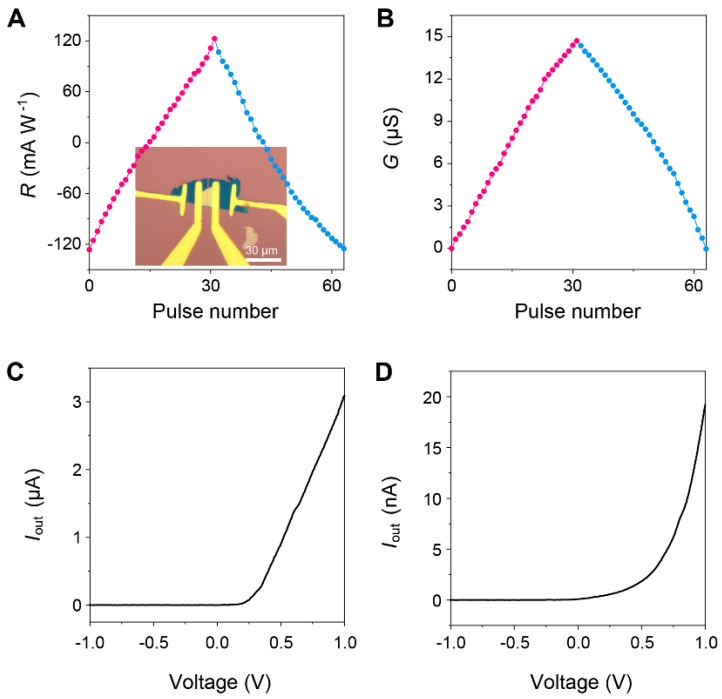


Fig. S65. Device performance of the Fe-FET fabricated with a P(VDF-TrFE) ferroelectric film. (**A**) Tunable photoresponsivity (*R*) under sequential programming pulses, exhibiting linear and symmetric switching between ±120 mA W^{-1}. Inset: optical image of the P(VDF-TrFE)-based device. (**B**) Conductance update as a function of pulse number, showing highly linear and symmetric updating behavior. (**C**) *I–V* curve exhibiting ReLU-type behavior when configured for a low junction barrier. (**D**) *I–V* curve showing Sigmoid-like nonlinear activation when programmed to a higher junction barrier state. These results confirm that the P(VDF-TrFE)-based Fe-FET reproduces the reconfigurable functionalities of ISC, IMC, and NAFs, validating the material generality of the proposed concept.

Table S1. Comparison of key parameters of ferroelectric devices.

Structure	$V_{programming}$	Switching speed	Energy consumption	On/Off ratio	Endurance	Retention	Reconfiguration flexibility	Ref.
Al/PVDF/Pt	±20 V	5 μs	0.24 fJ	N/A	10^6	10^4 s	IMC	Feng et al., 2025 (65)
Gr/Al_2O_3/2D ICE/Al_2O_3/Gr	±25 V	1 μs	N/A	10^6	10^4	N/A	Memory	Chin et al., 2021 (78)
CIPS/Gr/BN/MoS_2	±10 V	100 ns	N/A	10^7	10^4	10^4 s	Memory	Wang et al., 2021 (68)
0D WS_2	±10 V	140 ns	N/A	10^2	100	5×10^3 s	Memory	Niu et al., 2023 (79)
Gr/CIPS/Cr	-5.5V/4.5V	10-50 μs	N/A	10^7	10^6	8 h	Memory	Wu et al., 2020 (80)
PZT/LSMO/LAO	±3 V	50 ns	N/A	10^4	2×10^8	10^4 s	Synapse[a)]	Zhao et al., 2024 (81)
Fe/$BiFeO_3$/$La_{0.7}Sr_{0.3}MnO_3$/$SrTiO_3$	±3 V	10 μs	5 fJ	N/A	10^8	4 months	ISC	Guo et al., 2013 (82)
Au/Al_2O_3/$Bi_2O_2Se_3$	±5 V	10 s	N/A	10^4	N/A	N/A	Sensor[b)]	Wang et al., 2023 (83)
Gr/$MoTe_2$/PVDF/Au	±18 V	2 s	N/A	10^5	N/A	12 h	Sensor	Wu et al., 2020 (84)
Au/HfO_2/α-In_2Se_3	±2 V	100 ms	N/A	N/A	N/A	N/A	Synapse	Liu et al., 2022 (85)
MoS_2/$Hf_xZr_{1-x}O_2$/HfO_2	6~8 V	4.8 ns	3.4 pJ	10^6	10^{13}	1000 s	IMC	Ning et al., 2023 (62)
Pt/PZT/SRO	±3.5 V	100 ns	1.77 nJ	N/A	10^9	24 h	ISC, Memory	Lin et al., 2025 (86)
MoS_2/HfO_2/TiN/HZO/TiN	±4 V	30 ns	3 fJ	10^7	10^{12}	10^4 s	IMC	Lu et al., 2024 (31)
BP/Al_2O_3/HfO_2/Al_2O_3	±18 V	20 ms	N/A	200	200	2000 s	ISC, Memory	Lee et al., 2022 (87)
WSe_2/Al_2O_3/HfO_2/Al_2O_3	-6 V/+8V	5 μs	N/A	N/A	N/A	1000 s	ISC	Zhou et al., 2023 (17)
Gr/BN/MoS_2/CIPS/MoS_2	-1.5 V/0.22 V	0.4 s	N/A	10^4	10^4	10^3 s	Synapse	Chen et al., 2025 (64)
WSe_2/BN/Gr/CIPS/Gr	±7 V	100 ns	2.89 pJ	10^7	10^4	10^4 s	ISC, IMC, NAFs	**This work**

$V_{programming}$: Voltage pulses for programming. N/A: Not available. [a)] "Synapse" indicates platforms capable of basic synaptic functionality but without IMC capability; [b)] "Sensor" indicates platforms capable of basic sensing functionality but without ISC capability.

Table S2. Key parameters and functionalities of reconfigurable devices.

Material	Reconfigurable functions									Endurance	Retention	Temperature	Scalability	Ref.
	Synapse mode			Sensor mode			Neuron mode							
	$V_{programming}$	Operation energy	Operation speed	$V_{programming}$	Operation energy	Operation speed	Mode	Operation energy	Operation speed					
$MoS_2/HZO/Al_2O_3$	±5 V, 100 μs	N/A	N/A	-	-	-	-	-	-	10^8	$>10^{12}$ s	300°C	-	Gao et al., 2025 (88)
$MoS_2/CIPS/MoS_2$	–1.5 V, 0.2 s	N/A	N/A	-	-	-	-	-	-	10^4	10^3 s	-	-	Chen et al., 2025 (64)
Mo/HZO/TiN/ ZrO_2/IGZO	4 V, 100 μs	N/A	N/A	-	-	-	-	-	-	10^8	$>10^3$ s	-	-	Kim et al., 2024 (89)
$SnSe_2/WSe_2/HfO_2$/ W/TiN/Si:HfO_2/TiN	±4 V, 100 μs	N/A	N/A	-	-	-	-	-	-	14	N/A	-	-	Kamaei et al., 2023 (90)
Si/TiN/HfO_2/SiO_2/p -Si	±4 V, 10 ns	N/A	N/A		-	-	-	-	-	10^5	$>10^3$ s	RT-85°C	2 × 2	Xu et al., 2024 (91)
$MoS_2/CuInP_2S_6$	–20 V 1 ms +20 V 4 ms	N/A	N/A	-	-	-	-	-	-	10^4	$>10^3$ s	RT-72.5°C	-	Xia et al., 2024 (92)
IGZO/P(VDF–TrFE)	–5 V 1 ms +4 V 1 ms	N/A	N/A	-	-	-	-	-	-	N/A	>1900 s	-	5 × 4	Chu et al., 2024 (93)
α-In_2Se_3/SnS_2	±60 V, 30 s	N/A	N/A	-	-	-	-	-	-	800	$>10^4$ s	80-700 K	-	Ci et al., 2025 (94)
MoS_2/HfO_2/TiN/ HZO/TiN	±4 V, 30 ns	N/A	N/A	-	-	-	-	-	-	10^{12}	10^4 s	-	4 × 4	Lu et al., 2023 (31)
$MoS_2/Hf_xZr_{1-x}O_2/HfO_2$	±8 V, 4.8 ns	N/A	1 ns	-	-	-	-	-	-	10^{13}	10^3 s	85°C	8 × 3	Ning et al., 2023 (62)
$MoTe_2$	V_g –5~5 V V_d ±20 V	N/A	N/A	-	-	-	-	-	-	500	36 h	-	-	Peng et al., 2023 (95)
$Hf_{0.5}Zr_{0.5}O_2/SiO_2$	+5V, 500 ps	N/A	N/A	-	-	-	-	-	-	10^7	10^5 s	120°C	-	Wang et al.,

	–3.5V, 500 ps													2024 (96)
$LiNbO_3/HfO_2/MoS_2$	–2.3V, 10 s	N/A	N/A	±1.5 V, 15 s	N/A	N/A	-	-	-	40	10^3 s	-	3 × 3	Wang et al., 2024 (97)
$MoTe_2$/P(VDF-TrFE)	±35 V, 10 ms	N/A	N/A	±25 V, 10 μs	Self-power	1.9 μs	-	-	-	10^6	10^6 s	-	3 × 3	Wu et al., 2023 (30)
$WSe_2/Al_2O_3/HfO_2/Al_2O_3$	±6 V, 5 μs	N/A	N/A	N/A	Self-power	5 μs	-	-	-	N/A	10^3 s	-	3 × 3	Zhou et al., 2023 (17)
$Pt/Pb(Zr_{0.2}Ti_{0.8})O_3/SrRuO_3$	±3.5 V, 0.5 μs	1.77 nJ	10 μs	±10 V, 100 ns	Self-power	30 μs	-	-	-	10^9	24 h	-	2 × 2	Lin et al., 2025 (86)
α-In_2Se_3/HfO_2	–3 V, 1 μs	N/A	N/A	±5V, 8 s	N/A	N/A	-	-	-	10^4	N/A	-	3 × 3	Duong et al., 2024 (98)
PZT/SRO/STO	–1.94 V, 10 μs +1.89V, 10 μs	N/A	2.6 μs	±3 V, 0.15 ms	Self-power	1 ns	-	-	-	10^6	24 h	-	3 × 3	Cui et al., 2022 (99)
Gr/3R-WS_2/Gr	±2 V, 0.5 ms	N/A	N/A	±0.05 V, 1 s	Self-power	19.2 μs	-	-	-	2000	10^3 s	-	3 × 3 × 3	Gong et al., 2025 (100)
$BP/Al_2O_3/HfO_2/Al_2O_3$	–4 V~12 V 20 ms	N/A	N/A	±18 V, 20 ms	N/A	N/A	-	-	-	200	2000 s	-	3 × 4	Lee et al., 2022 (87)
CeO_2/STO	±10 V, 0.5 s	N/A	N/A	±10 V, 0.5 s	N/A	10 ns	-	-	-	100	1000 s	-	3 × 3	Li et al., 2025 (101)
SWNT@GDY	±0.5 V, 1 ms	N/A	N/A	±0.5 V, 1 ms	N/A	5 ms	-	-	-	10^5	10^4 s	-	3 × 3 × 3	Zhang et al., 2023 (16)
PEDOT:PSS/perovskite/C60/bathocuproine	±4 V, 10 s	N/A	N/A	±4 V, 10 s	3.63 fJ	2.75 ns	-	-	-	N/A	N/A	-	64 × 64	He et al., 2025 (35)
TiO_x/ZnO	±3.5 V, 100 ns	N/A	N/A	±3.5 V, 100 ns	N/A	N/A	-	-	-	10^9	5000 s	85°C	128 × 8	Huang et al., 2025 (36)
VO_2/Al_2O_3	-	-	-	-	-	-	ReLU	199.5 pJ	65 ns	5000	N/A	-	-	Oh et al., 2021 (52)
μ-Si multimodal	-	-	-	-	-	-	ReLU	N/A	N/A	-	-	-	-	Surekcigil

transistor														Pesch et al., 2022 (50)
TaO_x memristor circuit	-	-	-	-	-	-	ReLU, Sigmoid Tanh	N/A	N/A	-	-	-	-	Li et al., 2020 (53)
p(V3D3-co-VI)/ Al_2O_3 neural circuit	-	-	-	-	-	-	ReLU	0.5 pJ	N/A	-	-	-	-	Oh et al., 2023 (51)
MoS_2/CNT	-	-	-	-	-	-	Sigmoid	60 nW	N/A	-	-	-	-	Yan et al., 2023 (54)
WSe_2/BN/Gr/ CIPS/Gr	±3 V, 100 ns	64 fJ	< 8 ns	±3 V, 100 ns	Self-power	440 ns	ReLU Sigmoid	16fJ (ReLU) 80 aJ (Sigmoid)	8 ns	10^4	10^4	298-320 K	3 × 3 × 3	**This work**

$V_{programming}$: Voltage pulses for programming. N/A: Not available. "-": No such feature.

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